**ANNAMACHARYA UNIVERSITY FACULTY DETAILS FOR WEBSITE**

**About Profile**

NAME: **Mrs. P Syamala Devi**



PHOTO

DATE OF BIRTH: 1978-07-15

DESIGNATION: ASSISTANT PROFESSOR

DEPARTMENT: ECE

EMAIL ID: syamuvlsi@gmail.com

DATE OF JOINING: 17-04-2008

EMPLOYEE ID: [AITS041009](javascript:void(0))

## Academic Profile

| **Qualification** | **Name of the Board/University** | **YEAR** |
| --- | --- | --- |
| **M.Tech(VLSI)** | Annamacharya Institute of Technology and Sciences, Rajampet  **(affiliated by JNTUA)** | **2008** |
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## Research Details

1. Areas of Specialization: **VLSI**
2. List of Publications: **12**
3. Awards Received :
4. Research Guidance:
5. No. of PhD Guided:
6. No. of M.Tech Guided:**5**
7. No. of B.Tech Guided: **20**
8. Details of Professional Membership:
9. Subjects Taught:

**Satellite Communications**

**Analog Circuits**

**Antennas and Wave Propagation**

**Microwave Engineering**

**Electronic Devices and Circuits**

**Signals and Systems**

**Hardware description Language**

**Universal Human values**

**VLSI Design**

**ECA**

**DDTV**

**EMTL**

**ADICA**

**PDC**

**FPGA Architecture and its applications**

**DSP**

## Publication Details

|  |  |  |
| --- | --- | --- |
| **Title** | **Publisher** | **Published Year** |
| An Energy-Efficient 8-Tap FIR Filter Design in 22nm DTMOS Technology | Book chapter | 2025 |
| Performance Comparison of 4T SRAM Cell Using Different Techniques at 32nm and 22nm Nodes for Portable Electronic Devices | Book chapter | 2025 |
| Design and analysis of low power high speed SBFF and MBFF for signal processing applications | Scopus | 2024 |
| Design of 4-Bit Synchronous Counter Using TSPC-SVL T Flip-Flop for Power Reduction | IEEE | 2024 |
| Low Area-High Speed Architecture of Efficient FIR Filter Using Look Ahead Clock Gating Technique | Book chapter | 2023 |
| Design of High Efficiency FIR Filters by Using Booth Multiplier and Data-Driven Clock Gating and Multibit Flip-Flops | Book Chapter | 2023 |
| DESIGN AND SIMULATION OF STATUS REGISTER USING MULTIBIT FLIPFLOP FOR UART APPLICATION | UGC | 2018 |
| The design and Simulation of Split Radix FFT Processor using Multi-Bit FlipFlop for power reduction | UGC | 2017 |
| IDesign and optimization of Fir Filter using Multi-Bit Flip-flop | UGC | 2016 |
| Design and simulation of low power approximate adders using different technologies | UGC | 2014 |
| FPGA Based Real Time Implementation of Modified Tollgate System | UGC | 2013 |
| an efficient Dynamic Approach for Exact Reconstruction for CT Image Application | UGC | 2012 |

## Patent Details

| **Sno.** | **Title of Patent** | **Submitted/Published/Awarded** |
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