ANNAMACHARYA UNIVERSITY

About Profile

NAME: **Dr. SHAIK KARIMULLAH**

DATE OF BIRTH: **21-05-1988**

DESIGNATION: **Assistant Professor**

DEPARTMENT: **ECE**

EMAIL ID: munnu483@gmail.com, skr@aitsrajampet.ac.in

DATE OF JOINING: **15-06-2012**

EMPLOYEE ID: **AITS041023**

Academic Profile

Qualification	Name of the Board/University	YEAR
Ph.D	JNTUA, Ananthapuramu	2022
M.Tech	JNTUA, Ananthapuramu	2011
B.Tech	JNTUA, Ananthapuramu	2009

Research Details

1. Areas of Specialization: VLSI, Digital Image Processing, Bio-Medical Image Processing,

2. List of Publications: 65
Journals: 23, Conferences: 39, Books: 03

3. Awards Received: 00

4. Research Guidance:

A) No. of Ph.D Guided: **02** (Guiding)
B) No. of M.Tech Guided: **07**
C) No. of B.Tech Guided: **20**

5. Details of Professional Membership:

- Life Member-Indian Society for Technical Education, India
- Life Member-Institution of Engineers India

6. Subjects Taught:

Pulse and Digital Circuits, Digital Image Processing, Cellular Mobile Communications, Optical Fiber Communication, Design Thinking and Innovation, Signals and Systems, Analog Communication, Digital Communication, Electromagnetic Waves and Transmission Lines, Electronic Devices and Circuits, Radar Engineering, Nano Electronics

Publication Details

S.No.	Title	Publisher	Published Year
1.	An integrated method for detecting lung cancer via CT scanning via optimization, deep learning, and IoT data transmission	Frontiers	2025

2.	Improvised Spectral Efficiency and Channel Estimation Parameters in Visible Light Vehicular Communication by Integrating Simulation of Urban Mobility Data	IEEE	2025
3.	Blockchain-Enhanced Convolutional Neural Networks for Efficient Detection of Cardiovascular Abnormalities	Taylor & Francis	2024
4.	Pin density technique for congestion estimation and reduction of optimized design during placement and routing	Springer	2023
5.	An improved harmony search approach for block placement for VLSI design automation	Hindawi	2022

Patent Details

S. No.	Title of Patent	Submitted/Published/Awarded
1	Method for Improving Machine Learning Model Performance with Generative Adversarial Networks	Published
2	Method for Improving Machine Learning Model Performance with Generative Adversarial Networks	Published
3	VLSI Layout Using Redundant Nodes to Increase the Reliability	Published
4	A Machine Learning Based System for Physical Attack Protection for VLSI Chip Level Hardware Security and Method Thereof	Published
5	A System for Super Large-Scale Integration VLSI Method Thereof	Published
6	A Cloud Computing System for Optimizing Virtual Machine Placement and Configuration and Method Thereof	Published
7	A Novel Method and System for Designing VLSI Circuitry to Optimize the Integrated Circuit Operation	Published
8	A Novel Method of Power Reduction in Modified AES using Bit Encryption and Decryption Transition Scheme on FPGA	Published
9	A Novel Method of Design of Low Power VLSI Based Viterbi Decoder using Gate Diffusion Input	Published
10	Computer Implemented Method and System for Processing Qualitative Imaging to Detect and Forecast Abnormalities	Published
11	Computer Implemented System for Optimizing Placement and Routing in Very Large Scale Integrated Circuit Design	Published