



ANNAMACHARYA UNIVERSITY

EXCELLENCE IN EDUCATION; SERVICE TO SOCIETY
(ESTD, UNDER AP PRIVATE UNIVERSITIES (ESTABLISHMENT AND REGULATION) ACT, 2016)
Rajampet, Annamayya District, A.P – 516126, INDIA

Faculty Profile

Basic Information:

NAME : P SYAMALA DEVI
DESIGNATION : ASSISTANTT PROFESSOR
DEPARTMENT: ELECTRONICS AND
COMMUNICATION ENGG.
DATE OF BIRTH : 15-07-1978
DATE OF JOINING : 13-04-2007
EMAIL ID : syamuvlsi@gmai.com
EMPLOYEE ID : 63



Academic Profile:

Qualification	Name of the Board/University	YEAR
Ph.D.	VELTECH DEEMED TO BE UNIVERSITY, CHENNAI, TAMILNADU.	PURSUING
M. Tech	JNTU, HYDERABAAD	2008
B. Tech	JNTU, HYDERABAAD	2005

Research Details:

1. Areas of Specialization	:	VLSI DESIGN
2. No. of Publications	:	15
3. Awards Received	:	
4. Research Guidance		
	No. of PhD Guided:	-
	No. of MTech. Guided:	6
	No. of B.Tech. Guided:	20
5. Details of Professional Membership:		
6. Subjects Taught	:	EDC, ECA, SS, PDC, EMTL, PDC, STLD, AWP, MWE, DSP, DSPA&A, VLSI ESIGN, VLSIT, DSD, FPGA & A, SC, DDTV L, HDLP, UHV-II



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Publication Details:

Title	Publisher	Published Year
An Energy-Efficient 8-Tap FIR Filter Design in 22nm DTMOS Technology	SPRINGER	2025
Performance Comparison of 4T SRAM Cell Using Different Techniques at 32nm and 22nm Nodes for Portable Electronic Devices	SPRINGER	2025
Design and analysis of low power high speed SBFF and MBFF for signal processing applications	ELSEVIER	2024
Design of 4-Bit Synchronous Counter Using TSPC- SVL T Flip-Flop for Power Reduction	IEEE	2024
FinFET Based Design and Performance Analysis of Full Adders	IEEE	2024
Design of QCA-Based 1-Bit Magnitude Comparator	SPRINGER	2023
Low Area-High Speed Architecture of Efficient FIR Filter Using Look Ahead Clock Gating Technique	SPRINGER	2023
Design of High Efficiency FIR Filters by Using Booth Multiplier and Data-Driven Clock Gating and Multibit Flip-Flops	SPRINGER	2023

Patent Details:

Title of Patent	Submitted/Published/Awarded
IOT-BASED AUTOMATIC VEHICLE TRACKING DEVICE	INTELLECTUAL PROPERTY, INDIA