Faculty Profile

NAME	:	**Dr.M.Hanumanthu**
DESIGNATION	:	**Asst.Prof.**
DEPARTMENT	:	**ECE**
DATE OF BIRTH	:	**26-08-1984**
DATE OF JOINING	:	**04-06-2011**
EMAIL ID	:	**mhanumanth@gmail.com**
EMPLOYEE ID	:	**75**

Basic Information:

Academic Profile:

Qualification	Name of the Board/University	YEAR
Ph. D	NEC University, Nagaland	2025
M.Tech	JNTUA	2011
B.Tech	JNTUH	2005

Research Details:

1. Areas of Specialization	:	VLSI DESIGN
2. No. of Publications	:	18
3. Awards Received	:	NIL
4. Research Guidance		
	No. of PhD Guided:	NIL
	No. of MTech. Guided:	05
	No. of B.Tech. Guided:	24
5. Details of Professional Membership:		IFERP
6. Subjects Taught	:	VLSI, Digital Logic Design, Advanced digital design Concepts, Digital Communications Systems, Digital signal Processing, Electronic Devices and Circuits, Analog circuits, Digital Communications, HDL programming Language, Hardware software codesign, Algorithms of VLSI Design Automation, Cellular Mobile Communications etc.....

Publication Details:

Title	Publisher	Published Year
IoT Object Based Product Sorting Machine	IEEE	2025
Hardware Efficient Realization of 128 bit Advanced Encryption Standard in FPGA	IEEE	2025
Industrial Fault Detection System Using IoT Based Arduino and Node MCU	SSRN	2025
Facemask Detection Using Bounding Box Algorithm Under COVID-19 Circumstances	Elsevier	2024
Design of a Highly Reliable Low Power Stacked Inverter-Based SRAM Cell with Advanced Self-recoverability from Soft Errors	Elsevier	2024
Design Challenges And Trade-Offs In Sub-Threshold VLSI Circuits For IoT Applications	Research Trends Journal	2023
Enhancing energy efficiency in IoT devices through sub-threshold VLSI circuits	Multiresearch Journal	2023
Advanced TCAM Design Using SRAM	IRAJ	2021
DESIGN OF SRAM MEMORY USING REVESIBLE AND GDI LOGICS	IJATEST	2021
Detection of Spinal Tuberculosis Using DTCWT	*IJER*	2019
Design and Comparative Analysis of Domino Logic Styles	IndJST	2016
Orthogonal Latin Squares Encoders and Syndrome Computation by Auto-Checking and Correcting	: IJIRCCE	2015
urdhava-tiryagbhyam sutra multipler implementing by reversible gate logic	IJVDCS	2014
An Efficient colour space conversion using xilinx system generator	PAIDEUMA Journal of Research	2012

Patent Details:

Title of Patent	Submitted/Published/Awarded
Self-Realibility Based Weighted Soft-Bit-Flipping Algorithm for Decoding EG-LDPC Codes	Published