Unit-V

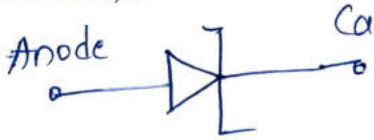
Special purpose devices-

Topics :-

→ Zener diode characteristics, zener diode as voltage Regulator
→ SCR diode
→ Tunnel diode
→ UJT
→ Varactor diode
→ Photo diode
→ Solar cell
→ LED
→ Schottky diode.

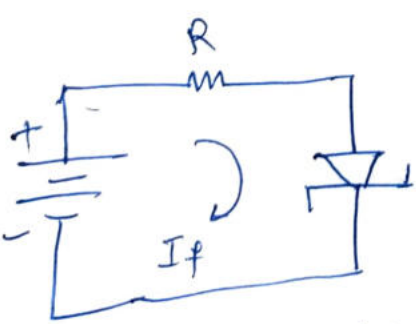
} All principles and operations of diode

* **Zener diode :-** Zener diode is a heavily doped PN junction diode. which is operated in breakdown region. Due to higher temperature and current capability Silicon is preferred in Comparision to Germanium.

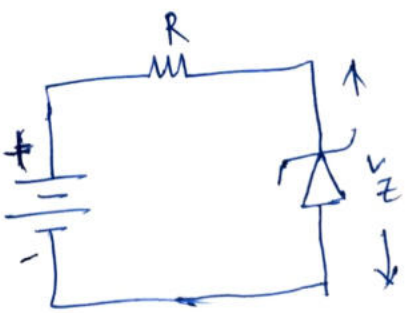


Symbol of zener diode

Fig(i)



fig(ii) Forward biasing zener diode



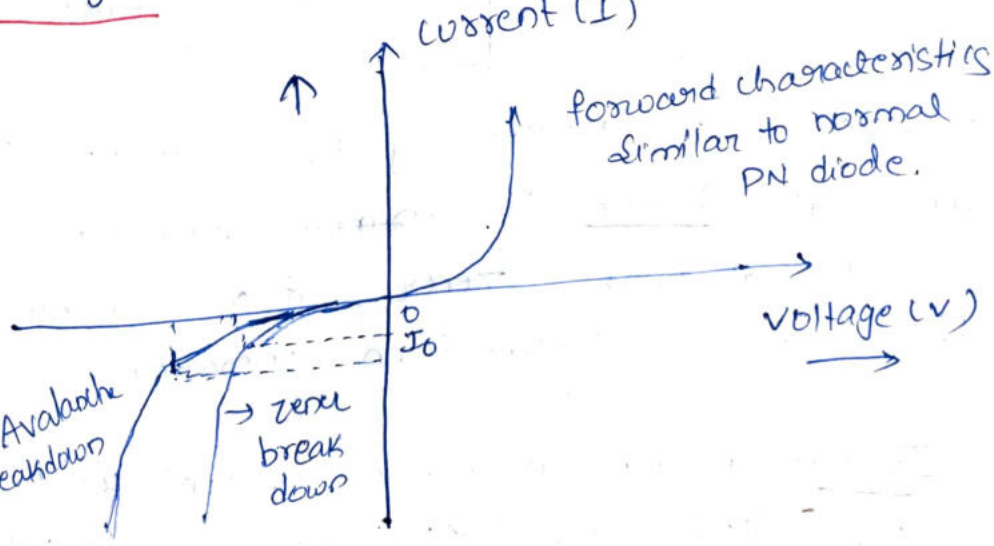
fig(iii) Reverse biasing zener diode

Fig (ii) represent forward biasing of ~~PN~~ zener diode it acts similar to PN diode in forward biased. Fig (iii) shows the reverse biasing of zener diode But in reverse biased it operated in reverse breakdown region.

→ In reverse biased, reverse current of zener diode limited using a series resistance then power dissipation at junction is limited to such a level which will not a damage the diode. and zener diode continous to operate safely in reverse breakdown region.

VI characteristics of zener diode :-

this work efficiently in reverse bias conditions. when reverse voltage increase beyond the breakdown voltage the current increases greatly from its normal cutoff value this voltage is called zener voltage or breakdown voltage.



The breakdown occur due to Zener breakdown or Avalanche Breakdown.

Zener breakdown	Avalanche breakdown
1. Breakdown due to intrinsic electric field across the junction	→ Breakdown due to collision accelarated charige carrier with adjacent atoms due to carrier multiplication
→ It occur for zener with zener voltage less than 6V	→ It occur for zener with zener voltage greater than 6V
→ Temperature coefficient is negative	→ Temperature coefficient positive
→ Breakdown voltages decreases junction tem perature increases	→ Breakdown voltage increases as junction Temperature increasey
→ VI characteristis is very shar in Break down Region	→ V-I characteristics not as sharp as zener breakdown

→ For zener diode, practically two currents are specified $I_{Z min}$ is ~~minum~~ minimum current through zener diode maintain its reverse break down operation

→ $I_{Z max}$ is the maximum current which zener diode can take. Safely maintaining its reverse breakdown operation ie Constant

V_Z crossit. If reverse current exceed this value, diode may get damage due to excess power dissipation.

→ zener diode is most suitable for voltage Regulation.

* Zener diode as voltage Regulator :-

→ zener diode used in its reverse biased region the current through the diode is very small of order of μA. when sufficient reverse bias is applied electrical breakdown occur the large current flows through it. Such a breakdown occur at a voltage called zener voltage V_Z. In this condition whatever may be current the voltage across the zener is constant i.e V_Z.

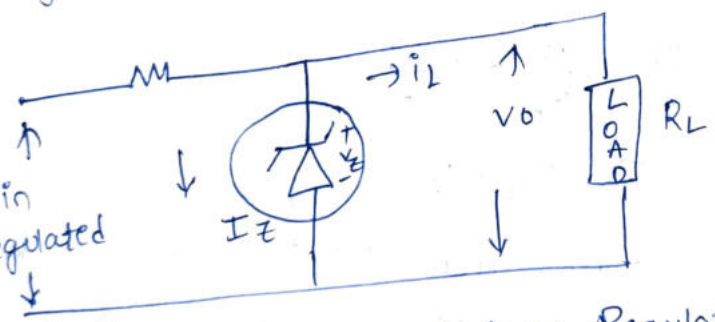
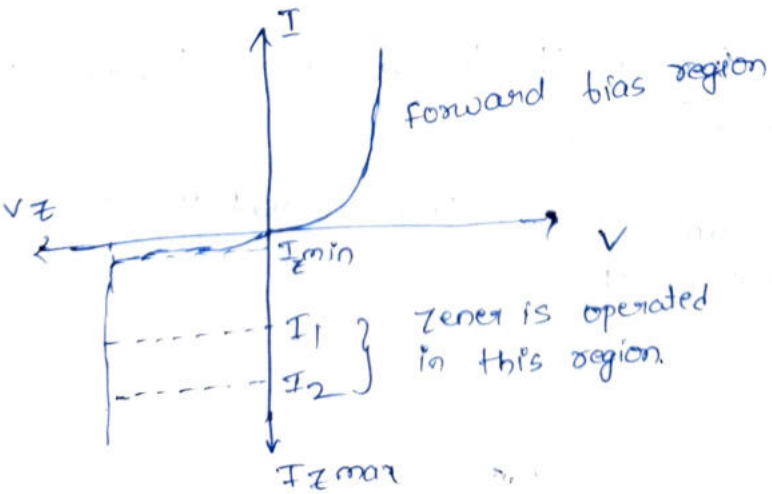
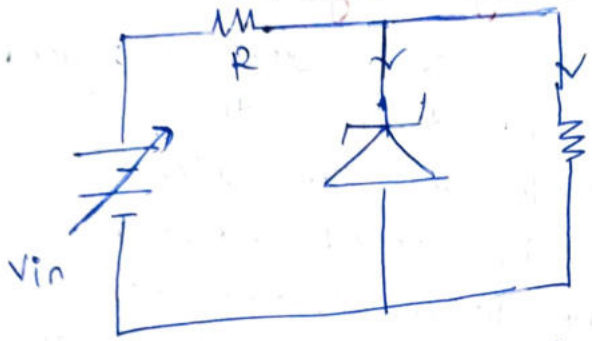


fig :- zener diode as Regulator



As the voltage across the zener diode is constant V_z. it is connected across the load and hence the load voltage is V_D is equal to zener voltage V_z

Regulation with Varying Input voltage :-



Zener Regulator.

Zener Regulator with Varying input voltage Regulation.

$V_0 = V_z$ is Constant

$$\therefore I_L = \frac{V_0}{R_L} = \frac{V_Z}{R_L}$$

and $I = I_Z + I_L$

As V_{in} increases then total current I increases But I_L is constant as V_z is constant hence the current I_z increases to keep I_L constant

As long as I_z in between I_{zmin} and I_{zmax} the V_z is V_D.

If V_{in} decreases then current I decreases but to keep I_L constant I_z decreases.

Analyzation of Zener regulator.

$$I_L = \frac{V_O}{R_L} = \frac{V_Z}{R_L}$$

The current through Zener must be I_{Zmin} to keep in reverse biased

$$I = I_L + I_{Zmin}$$

$$V_{in\,min} = V_Z + IR$$

$$V_{in\,max} = V_Z + IR \quad \text{since}$$

$$I = I_L + I_{Zmax}$$

The maximum power dissipation in Zener diode is given by

$$P_D = V_Z I_{Z(max)}$$

* Silicon controlled Rectifier:-

→ The SCR is unidirectional device and it allows flow of current in only one direction. But it has built in feature to switch 'on' and 'off'.

→ The SCR switching (on, off) is controlled by gate and biasing conditions.

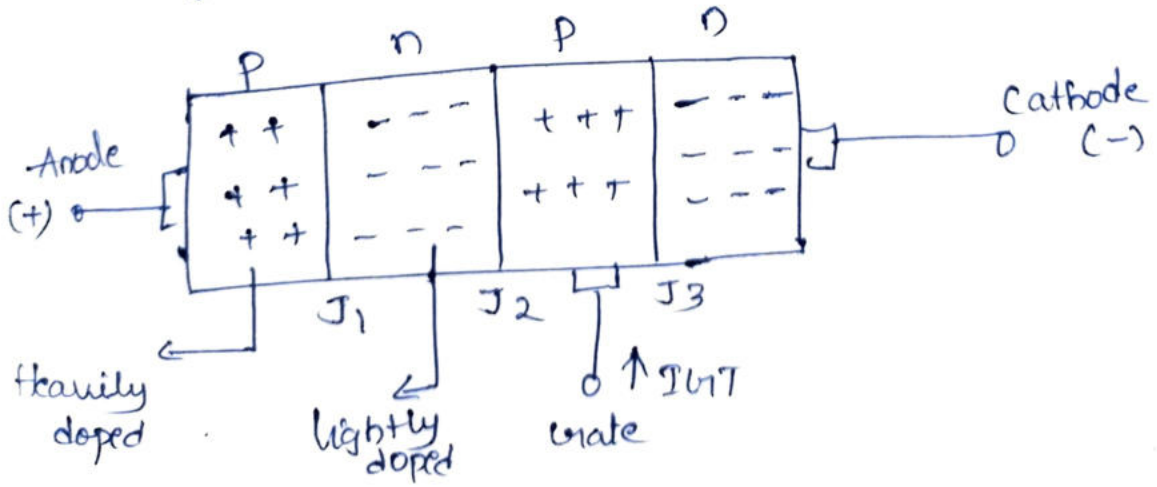
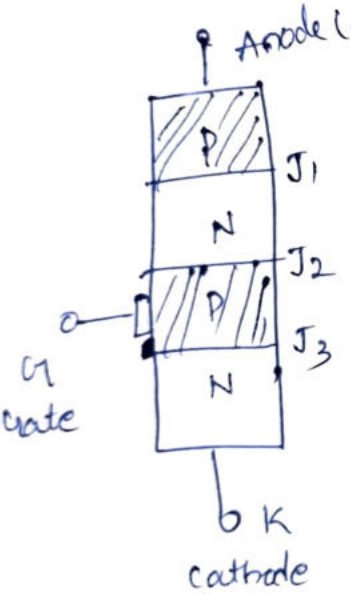


Fig (i) Construction of SCR

→ SCR is a four layer P-N-P-N device where P and N layers alternately arranged. The outer layer are heavily doped.

→ There are three pn junctions called J_1, J_2, J_3. The outer P-layer is called anode. while outer N-layer is called cathode. the middle layer is gate.

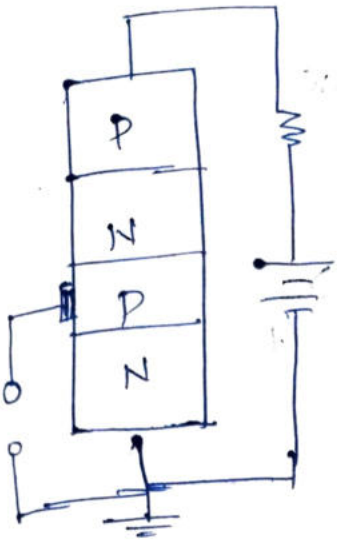
→ Anode and cathode are not sufficient to turn 'ON' SCR. To make it ON, a current is to be passed through this gate terminal denoted as I_{GT}. Thus SCR is current operated device.



symbol

Operation: Case(i) gate is open
In SCR a load is connected in series with Anode and kept positive with respect to cathode. the operation of SCR can be Studies when the gate is open.

→ when the gate is open no voltage applied at the gate then J_1 and J_3 are forward biased while J_2 reverse biased



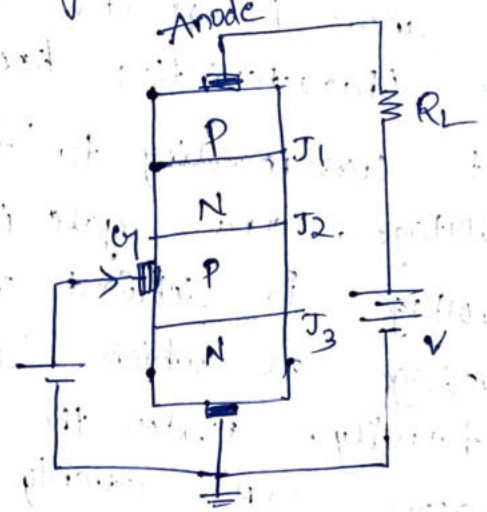
fig(i) gate is open

→ Due to reverse bias of junction J_2 no current flows through R_L and hence SCR is cutoff when anode voltage increased beyond critical value. then Junction J_2 breakdown

→ Now SCR conduct heavily and said to be ON. Hence SCR offer little forward resistance.

(ii) Applying voltage at gate terminal.

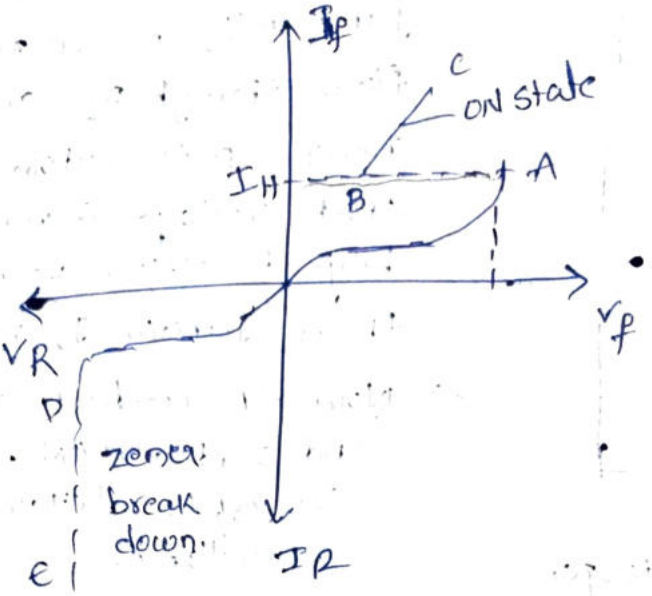
+ when the gate is positive w.r.t cathode J_3 is forward bias. while J_2 is reverse bias electrons from N-type move across junction J_3 towards gate, while hole from p-type move across junction J_3 towards cathode.



So gate current start flowing In once SCR Starts conducting the gate loses all control the current keeps flowing indefinitely. Untill circuit is open.

VI characteristics:-

VI characteristics in forward bias condition drawn between V_f and I_f. Reverse bias Condition drawn between V_r and I_r.



→ VI characteristics of a SCR for $I_{GK}=0$ when the anode is positive w.r.t to cathode. the characteristics known as forward characteristics volt corresponding to 'A' is called forward voltage, and gate is open the breaker voltage is defined as minimum forward voltage at which SCR start conducting heavily. Under the condition voltage across SCR suddenly drops as shown by dotted curve AB. The current corresponding to point B is I_H and is known as holding current.

Reverse characteristics: Anode to cathode voltage is reversed then device enter into reverse blocking region. the current is negligible small & practically neglected.

→ If reverse voltage increases similar to diode at particular value avalanche breakdown occur and large current

flows through device called reverse breakdown.
→ forward breakover voltage greater than reverse breakover voltage.

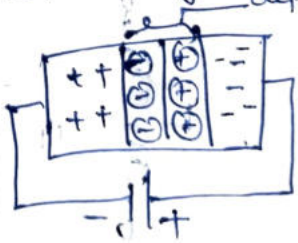
Advantages :-
→ Very small amount gate drive required.
→ SCR with high voltage and current ratings available.

disadvantages :-
→ Gate has no control, once SCR turned ON.
→ operating frequency are low.

* Varactor diode :-

→ It is also named as variable capacitor, varicap (or) voltage variable capacitor, Tuner circuit.
→ Varactor diode are mainly preferred under reverse bias condition. it is also a junction diode with small impurity doping at its junction.
→ It has a usebul property that its junction/ transition capacitance is easily varied due to diode preferred for high frequency application.

fig :- Symbol.



→ When any diode is reverse bias, a depletion region will form. The larger reverse bias voltage is applied across the diode, the width of depletion Region become wider and by decreasing Reverse voltage become narrower.

Varactor diode :

1. Varactor diode acts like variable capacitor under Reverse bias condition.
2. Another names Varicap, Tuning, variable Reactance, variable capacitance diode
3. It is manifactured to show better transition capacitance property than ordinary diodes.
4. Symbol : 

. Two parallel lines at cathode represent two conductive plates and the space b/w two parallel lines represent dielectric
5. When we apply Forward bias voltage is applied, electric current flows through diode As result depletion Region become negligible. [Forward bias of PN diagram draw here
6. We know that depletion region consist of Stored charges. so stored charges become negligable which is undesirable.
7. Designing this to store charges not to conduct electric current.
8. when a Reverse bias voltage applied electrons from n-region & holes from p-region move away from junction. [R.B of PN draw here
9. As a Result, width of depletion Region increases and capacitance decreases
10. Applied Reverse voltage is low then capacitance is very large. | capacitance $\propto \frac{1}{\text{width of Depletion Region}}$
11). R.B voltage ↑ width of D.R ↑ capacitance ↓

12. the decrease in capacitance means decrease in storage charge. so reverse bias voltage kept at minimum to achieve large storage charge

13. Thus, capacitance varied by varying the voltage.

Fixed capacitor → capacitance will not varied

variable capacitor → capacitance varies

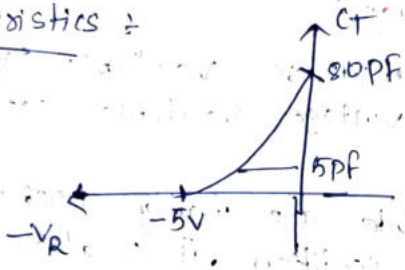
14. Units capacitance measured in picofarads(PF)

→ This depletion Region is constant consist of micority Carrier and act like insulator dielectric where as two p and n region will acts as plates forming a capacitor.

→ As the capacitance, is inversly proportional to distance between the plates; so the capacitance varies inversly with applied voltage.

i.e $C_T \propto \frac{1}{V_R}$

Characteristics :



Applications :

→ main application of Varactor diode is LC tuned circuit

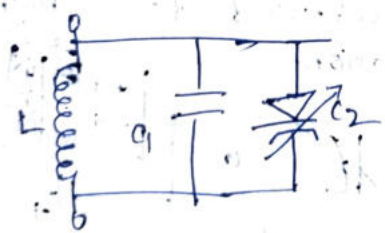


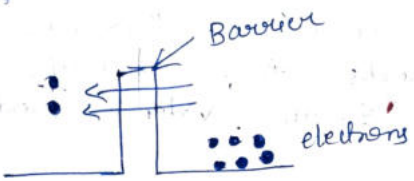
Fig :- Use of Varactor diode LC tuned circuit

Resonance frequency $(f_i) = \frac{1}{2\pi\sqrt{L(C_1+C_2)}}$

→ FM modulator
→ Automatic frequency control device
→ Adjustable band pass filter
→ television receivers.

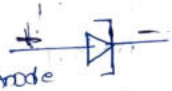
Tunnel diode :

1. Tunnel diode is a heavily doped PN junction diode in which electric current decreases as voltage increases.
2. The tunnel diode is used as very fast switching device in computer. It is also used in high freq oscillator and amplifiers.



→ meaning of Tunneling is moving

3. Symbol of Tunnel diode



→ It is mainly designed using Germanium material other than Germanium these diode are made up of Gallium Arsenide, Gallium Antimonide, Silicon.

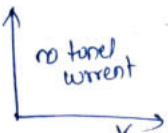
→ Anode is positively charged electrode which attracts electrons. Cathode is negatively charged electrode which emits electron

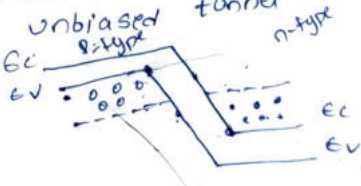
4. n-type semiconductor emits electron so it is refered to as cathode
p-type semiconductor attracts electron emitted from n-type semiconductor. so p-type referred as the anode

Working :

Case(i) :- Unbiased tunnel diode :-

→ when no voltage is applied to the tunnel diode. It is said to be an unbiased tunnel diode.





→ In a tunnel diode, conduction band of the n-type material overlaps with valency band of P-type material because of heavy doping.

→ Because of this overlapping the conduction band electrons at n-side and valence band hole at P-side are nearly at the same energy level.

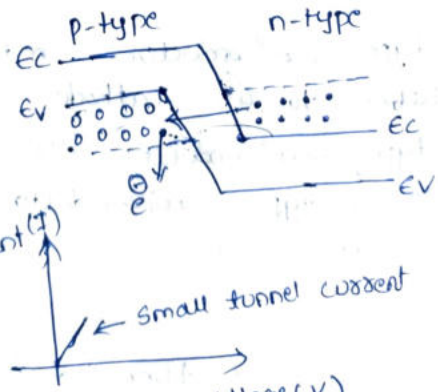
→ So. when the temperature increases, some electrons tunnels from conduction band of n-region to the valence band of P-region.

→ In a similar way holes tunnel from valency band of P-region to the conduction band of n-region

(case (ii)) :- Small voltage applied to tunnel diode

→ when small voltage applied to diode i.e less than (critical value (or) built in voltage of depletion layer no current flows through junction

→ Small no of $e^{\ominus}$ in conduction band will move to the empty state of valence band in p-region. This create small forward current



○ → hole

● → electron

C.B → conduction band

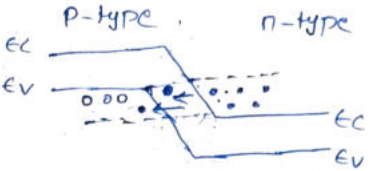
V.B valency band

(case iii) Applied voltage slightly increases.

→ when voltage to diode increases, large No of free e⊖, holes generated

→ voltage increases overlapping of conduction band & valency band is increased.

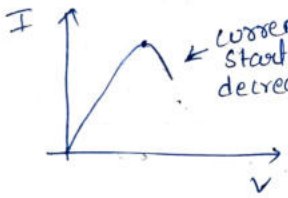
→ Energy levels of C.B & V.B are equal. maximum current flows

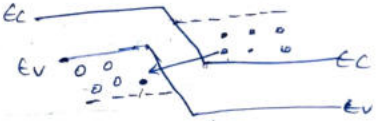


(case iv) Applied voltage further increased:-

If applied voltage is further increased, misalign of C.B & V.B takes place

→ e⊖ from conduction band move to V.B cause small current flow. tunneling current start decreasing





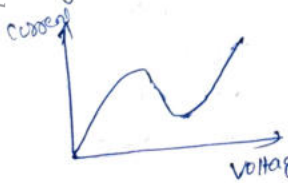
(case (v):- Applied voltage largely increased.

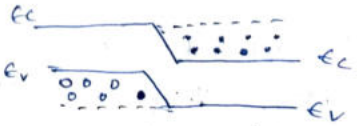
If applied voltage largely increases the tunneling current drop to zero.

→ At this point no longer overlap of C.B & V.B it work smilar to pn diode.

→ If applied voltage greater than built in potential current start flow through diode

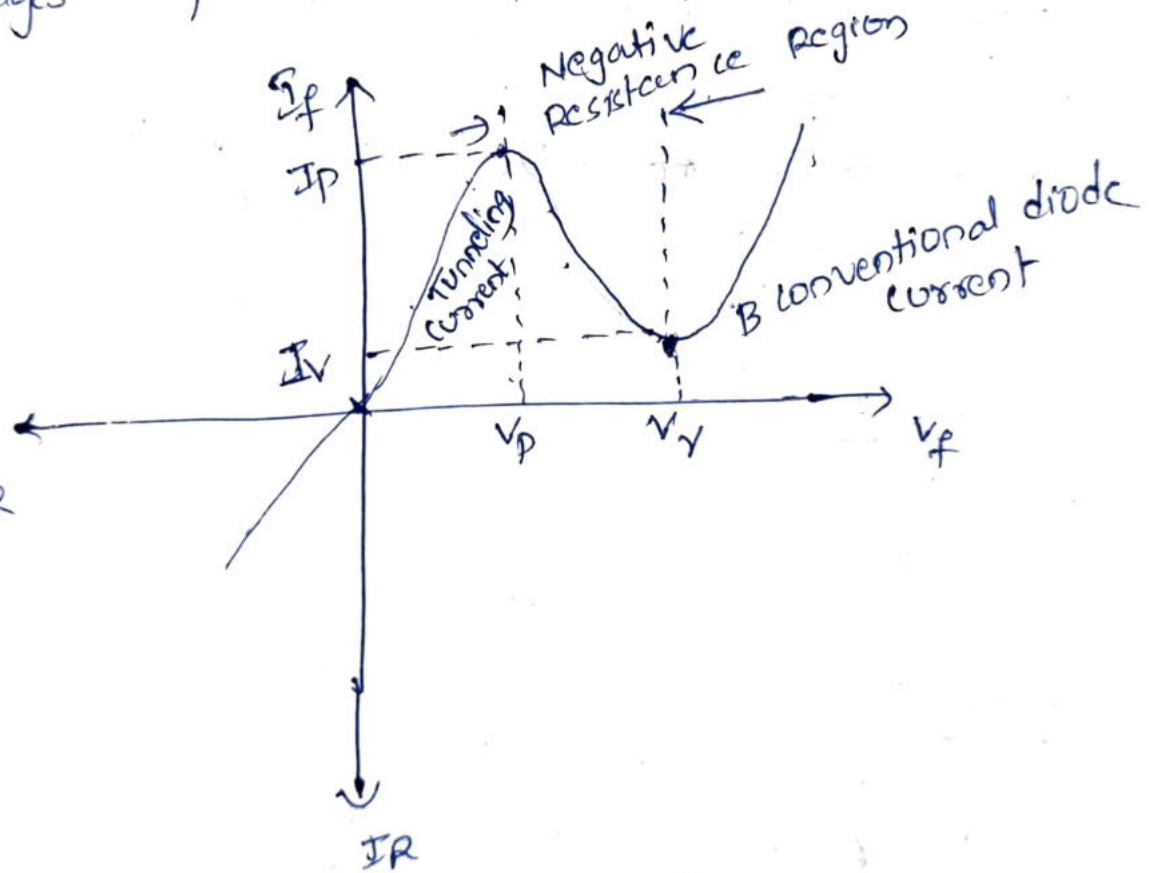
→ The portion of curve in which current decreases as voltage increases it is the negative resistance region of tunnel diode. used in amplifier & oscillator





VI characteristics :-

As soon as forward bias is applied significant current produced the current reaches its peak value I_p. when forward voltages reaches value V_p.



→ when forward voltage is further increased the diode current start decreasing thus reaches a point I_V corresponding to a valley voltage V_v.

The Region from point A to B is called as negative resistance region. For the voltages greater than V_v the current start raising as in case of normal PN junction diode.

Peak current point : (I_p) :

The voltage at which current flowing through tunnel diode reaches maximum value named as peak current (I_p).

Valley current (I_v) : The voltage which the tunnel diode current increases after a position of decrement and voltage at which tunnel diode is ready to work as p.n diode named as valley voltage and corresponding current is valley current.

Negative Resistance Region : This region present at particular interval between peak current to valley current. Region wher voltage is increasing but current decreases. i.e negative Resistance Region.

Advantages :

- Low cost
- Low noise
- Low power consumption

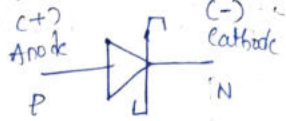
Applications :

- As high speed switch
- In computer logic circuits
- high frequency oscillators, amplifiers

* Schottky Diode :- → unipolar device

→ Schottky diode is a metal semiconductor junction diode that have less forward voltage drop (0.3-0.5) than PN junction diode and can be used in high speed switching application

→ Symbol of Schottky diode



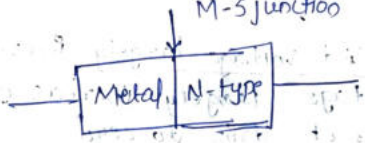
metal acts as anode and n-type semiconductor acts as cathode.

→ Metal like platinum & Aluminium replace the p-type semiconductor (Anode)

→ Another names of schottky diode are Schottky Barrier diode, Surface barrier diode, Majority carrier device, Hot electron diode

Construction :-

→ When Aluminum, platinum joined with n-type semiconductor. Junction formed between them is called M-S junction (or) metal semiconductor junction. (or) schottky barrier



→ Schottky diode can switch on and off much faster than PN diode

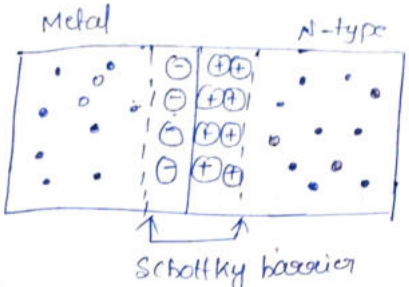
→ produce less unwanted noise than PN diode

→

Working :-

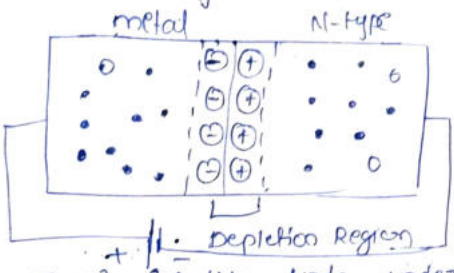
→ In a forward bias the electrons in N side gain enough energy to cross the junction barrier and move into metal with large energy they are called it hot carriers so diode is called as hot carrier diode.

Before applying a forward bias the $e^{\ominus}$ in N-side having less energy level than of metal so $e^{\ominus}$ cannot cross the junction barrier called schottky barrier



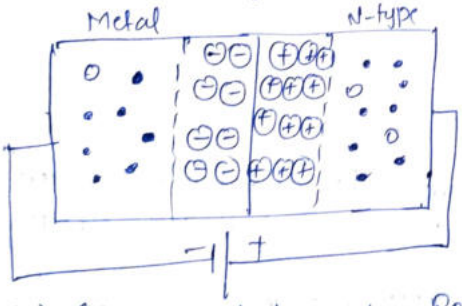
⊕ → positive ion
⊖ → Negative ion

Fig(i) Schottky diode under unbiased condition



• → free $e^{\ominus}$
o → free hole

Fig(ii) Schottky diode under forward bias condition



fig(iii) Schottky diode under Reverse bias condition

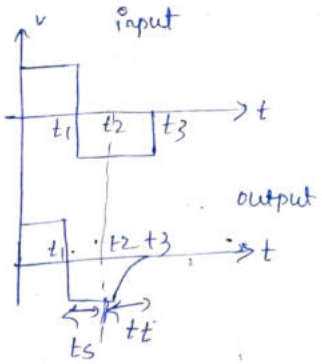
Reverse Recovery time :- (R.R.T)

⇒ the switching from conducting to non conducting state is called Reverse Recovery time.

⇒ R.R.T of schottky diode is less than the normal PN junction diode because in schottky diode no minority charge carriers.

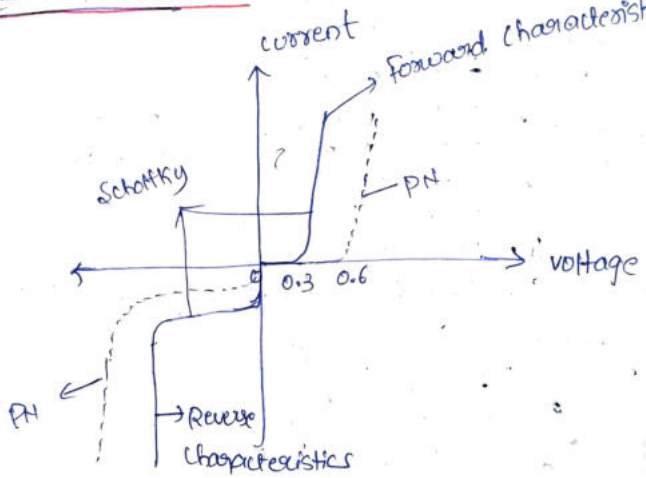
Reverse Recovery time $= t_s + t_r$

→ At time t_1 in output side it should become zero but some finite amount of current is flowing due to minority carriers this time is called storage time.



→ The time at which current start decreasing is called transition time.

VI characteristics :



----- dot indicate characteristics of PN junction
——— indicates characteristics of Schottky

→ Voltage drop of schottky diode range from 0.3 to 0.5 V

Example :

Normal diode

$I = 50A \quad V_f = 0.6V$

$P = V \times I = 50 \times 0.6V$

$P = 30W$

Schottky diode

$I = 50A \quad V_f = 0.3$

$P = V \times I = 50 \times 0.3V$

$= 15W$

Schottky diode discipate less power due to low voltage drop than normal diode.

Advantage:
→ less Recovery time
→ less voltage drop
→ low barrier potential

disadvantages:
→ high Reverse leakage current
→ low reverse voltage Rating

Applications:
→ switching circuits
→ RF mixers
→ Solar cell applications.

LED :- (Light Emitting Diode)

→ opto semiconductors called light emitting diodes (LEDs) it transfers electrical energy into light energy.
→ It lights up when we apply the voltages. it has longer life span than laser diodes.

Construction:-

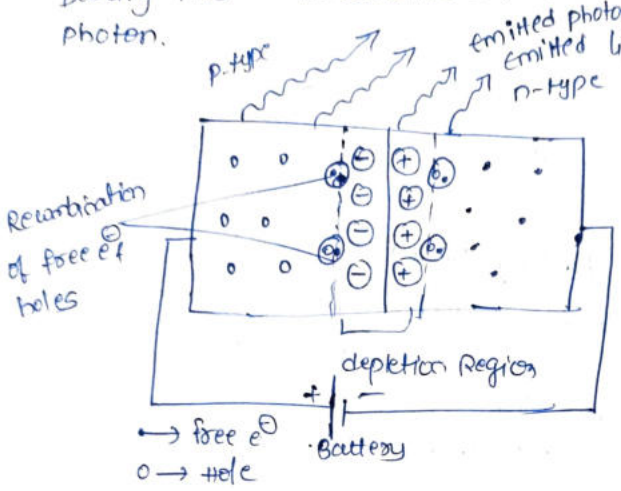
Same like PN junction diode LED also can allow current only in one direction i.e forward bias condition. P type material connected to +ve terminal and n-type material connected to -ve terminal of battery. LED consist of two terminals Anode & cathode.

fig(i) symbol of LED

→ Light being emitted by the diode. LEDs comes in variety of colour. like orange, yellow, green red LED are mostly available on LEDs
→ Symbol of LED does not Represent any colour
→ gallium, phosphorous, arsenic materials are used in construction.

LED working :

LED function only in forward bias condition holes in the psides & electrons in the n-side move towards the junction. $e^{\ominus}$ & recombine with hole. width of depletion Region reduce. During this Recombination produce light or photon.



Fig(i), working of LED

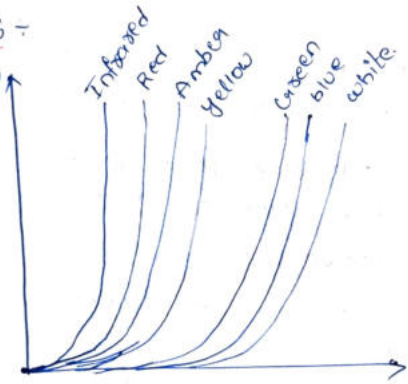
Before recombining with holes in valency band the free $e^{\ominus}$ in conduction band lose the energy inform of light. the gadget may damaged if reverse bias voltage applied to LED's. All diodes produce light (or) photons. but not all of them produce visible light. In just one millisecond LED can turn ON and off.

Colours of LED :

Exotic Semiconductor material such as gallium arsenide (GaAs), gallium phosphide (GaP), gallium arsenic phosphide (GaAsP), silicon carbide (SiC) (or) Gallium indium nitride (GaInN) used to make light emitting diode.

semiconductor material	wavelength	colour	(V_F) cut in voltage
GaAs	850 - 940nm	Infra-red	1.2V
GaAsP	630 - 660nm	Red	1.8V
GaAsP	605 - 620nm	Amber	2.0V
GaAsP-N	585 - 595nm	yellow	2.2V
AlGaP	550 - 570nm	Green	3.5V
SiC	430 - 505nm	Blue	3.6V
GaInN	450nm	White	4.0V

Characteristics :-



Advantages :-

→ long life.
→ energy efficiency
→ high brightness, Reliability

Disadvantages :-

→ Impact on insects
→ Temperature sensitivity
→ Electrical polarity
→ voltage sensitivity

Applications :-

→ used as bulb in homes & industries.
→ used in motorcycles & cars
→ traffic light signals

* Solar cell :-

→ Solar cell is commonly refered to as photo voltaic cell. It is a electrical device uses photo voltaic effect to transform light energy to electrical energy.

→ A photo electric cell is a type of device whose electrical properties, such as current, voltage or resistance, change in response to light.

→ Solar panels also knows as modules or solar cells are made up of individual solar cells.

Construction :-

→ Design of solar cell slightly different from PN junction diode in terms of manufacturing.

→ On the top of a thick N-type semiconductor, a very thin layer of P-type semiconductor is formed on bottom.

→ P-type semiconductor cover with few thinner electrodes.

→ The band gap of materials used to make solar cells must be close to 1.5 eV.

→ GaAs, CdTe, CuInSe are materials used in construction.

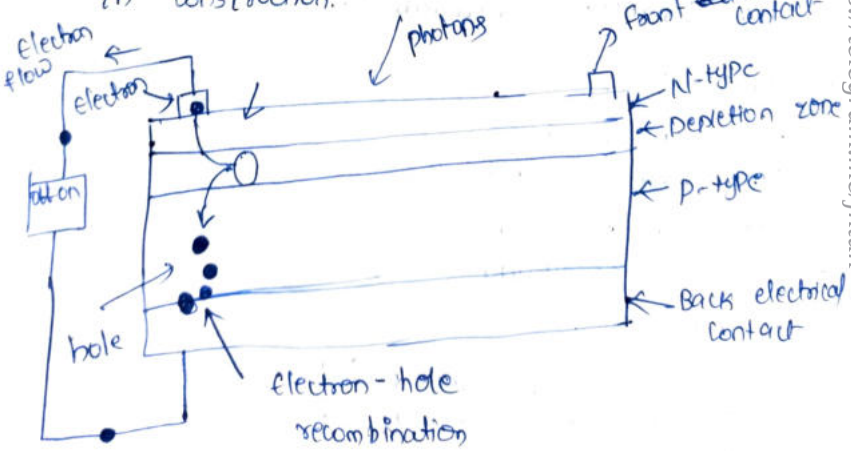


Fig Construction of solar cell

Working :-

→ Light photons easily pass through the incredibly thin p-type layer to enter the PN junction when light reaches.

photons from light source give the junction enough energy to make many $e^{\ominus}$ hole pairs.

The junction's thermal equilibrium condition broken by incident light

In depletion region free $e^{\ominus}$ move quickly to junction & N-type side. similarly p-type side of junction can be readily reached by hole.

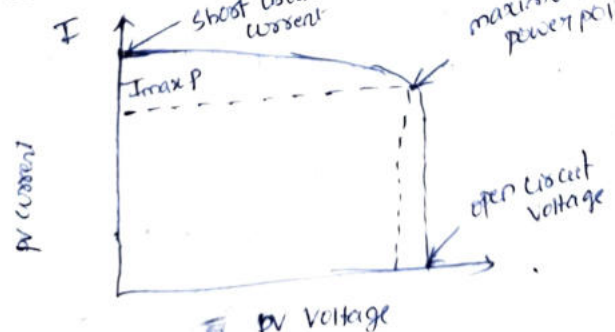
PN junction will act like miniature battery cell as concentration of holes increases on one side ie p-type side of junction. $e^{\ominus}$ increases on other side N-type side of junction.

→ A voltage known as photo voltage is set up.

V-I characteristics :-

→ x-axis represent photo voltage. y-axis represent photo current.

→ the photocurrent is at its greatest at zero photo voltage and it decline as photo voltage rise above zero. The term " highest power point " refer to voltage at which the photo current begins to decline



Advantage :-

→ No pollution associated with it.
→ It must last for long time
→ No maintaince cost

Disadvantage :-

→ It has hight cost of installation
→ It has low efficiency

Applications :-

→ Supply electricity for telecommunication repeater stations, water pumps, cottages

* photodiode :-

→ It transforms light energy into electrical energy very quickly
→ Another names photo detector, light detector, photo sensor. It operate under reverse bias condition

Types of photodiodes :-

a) PN photodiode :- It is first developed. it has poor sensitivity compared to other

b) PIN photodiode :- mostly widely used photo diode.

c) Avalanche breakdown :- Due to its high gain Levels, this type of diode utilise in low light environment

d) Schottky photodiode :- It is used in optical communication. it has low voltage drop.

Symbol of photodiode :-

Construction :-

→ P-type & N-type semiconductors can be used to create photodiode.

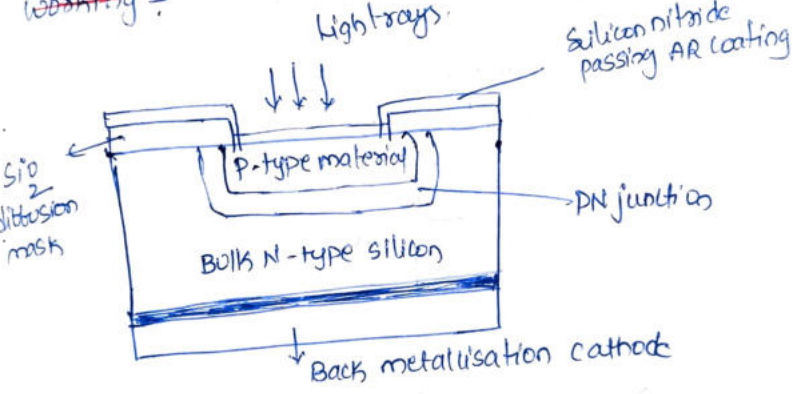
→ Diffusion of P-type substrate, which is midly doped. P+ ion layer formed due to diffusion

→ N-type epitaxial layer can form on N-type substrate.

→ Metals are used in the contact's construction to create two terminal that resemble an anode and cathode.

→ Active and non-Active surfaces present- non-Active surface prevents light rays from striking., but active surface allows light rays to pass across it.

Working :-

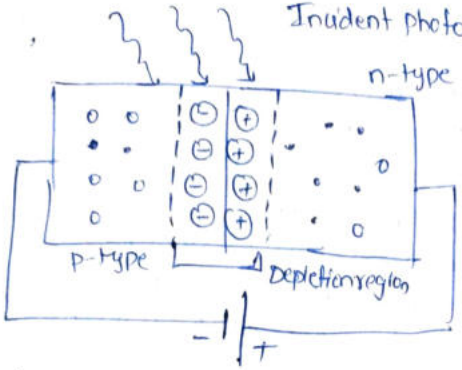


Working :-

→ when photon of light strike the diode it create hole & $e^{\ominus}$ recombination due to inner photoelectric effect.

→ carriers are move away from the junction

→ hole move towards cath The sum of photocurrent and absence of light make up total current flow through diode



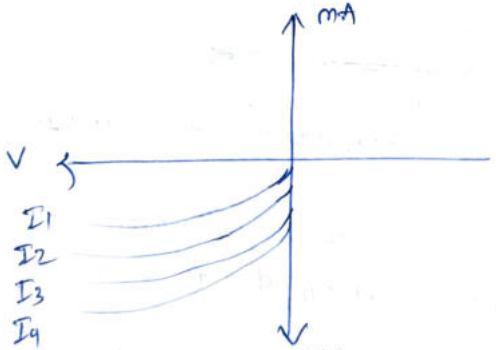
Modes of operation :-

Photovoltaic mode :- This refered as zerobias mode

Photo conductive mode :- width of Depletion region more with applying reverse voltage.

Avalanche breakdown :- operate with high reverse bias. breakdown occurs.

V-I characteristics :-



$I_4 > I_3 > I_2 > I_1$

→ photocurrent · Esentially unaffected by applying reverse voltage. with exception tiny dark current. Photo current is zero

→ photocurrent rises linearly along with optical power.

Advantages :

→ Less resistance
→ long life span
→ Less noise
→ loss weight

Disadvantages :

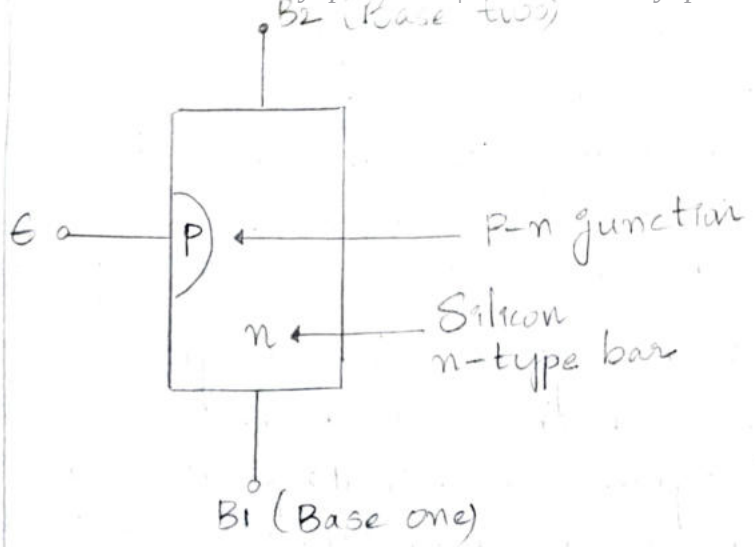
→ Temperature stability is poor
→ less sensitivity
→ It uses offset voltage

Applications :

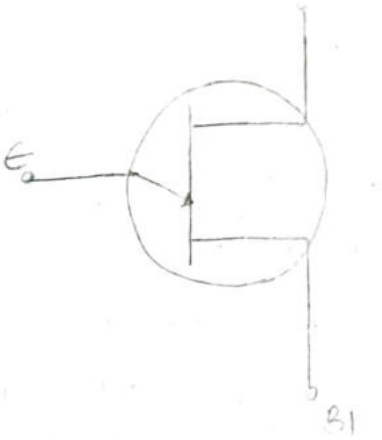
→ Smoke detector, Compact disc player, television
→ Photo conductor, photo multiplier tubes.
→ Used for lightning regulation and optical Communication.

UJT (Unijunction Transistors) :-

It is a three teaminal device having two layers
It consists of lightly doped n type silicon slab to which aluminium rod is alloyed at the one end with a p-type material, forming a p-n junction.
At other end of slab, two base contacts B1 and B2 are attached. The third teaminal emitter e is taken out from aluminium rod



Structure of UJT



Symbol of UJT

→ The fig shows the construction and symbol of UJT

→ It has only one p-n junction hence called Unijunction.

→ The p-n junction can be treated as a diode D while internal resistance of two bases are denoted as R_{B1} and R_{B2}. The resistance R_{B1} is greater than R_{B2}.

→ When emitter diode is not conducting, the resistance between two bases is called interbase resistance given by $R_{BB} = R_{B1} + R_{B2}$

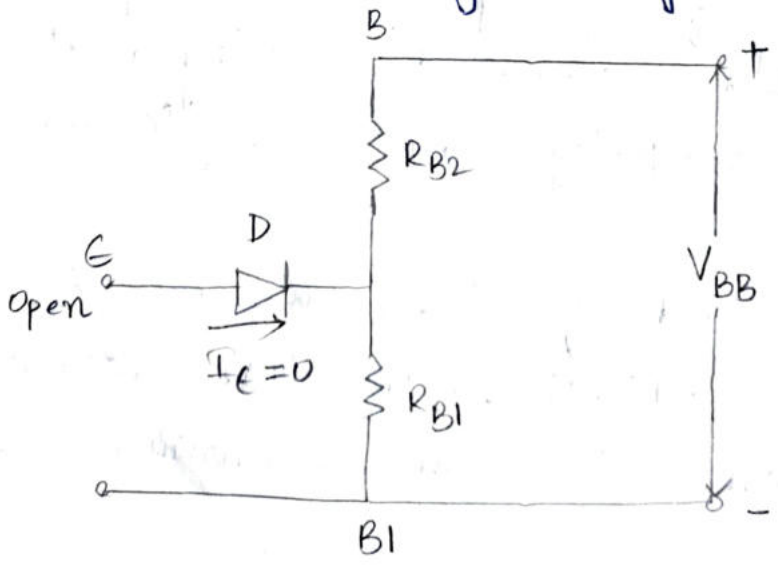


fig: Equivalent circuit of UJT

The fig shows the equivalent circuit of UJT When $I_E = 0$, then the voltage drop across R_{B1} is given by,

$$V_{RB1} = \frac{V_{BB} R_{B1}}{R_{B1} + R_{B2}} = \eta V_{BB}$$

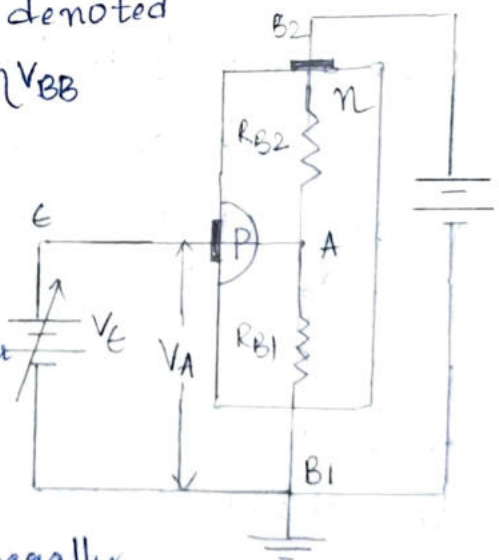
$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} \Big|_{I_E = 0} = \frac{R_{B1}}{R_{BB}} \Big|_{I_E = 0} = \text{Intrinsic stand off ratio}$$

∴ The value of η is between 0.5 to 0.8

Working of UJT:-

The supply voltage V_{BB} is connected between B_1 and B_2 while variable emitter voltage V_E is applied to emitter. This shown in the fig The V_E is used to forward bias the diode. The drop across diode is V_D.

The potential of A is denoted by η and is equal to ηV_{BB}



Case(i) $V_E < V_A$

As long as V_E is less than V_A the p-n junction is reverse biased. Hence emitter current I_E will not flow.

Case(ii) $V_E > V_P$

The diode drop V_D is generally between 0.3 to 0.7V.

Hence we can write

$$V_P = V_A + V_D = \eta V_{BB} + V_D$$

When V_E becomes equal to or greater than V_P the p-n junction becomes forward biased and current I_E flow.

→ Due to this the charge carriers are injected in the R_{B1} region of the bar.

→ Due to this additional charge carriers, the conductivity of the R_{B1} region increases i.e resistance and due to which the drop across it also decreases.

→ This makes the p-n junction more forward biased which further increases the current and more charge carriers are injected.

→ The current I_E is increases to a value determined by the source resistance.

→ Under these conditions, the UJT is said to be ON and remains in this condition till the input is open or the current I_E gets reduced to very low value.

UJT characteristics:-

→ The graph of emitter current against emitter voltage plotted for a particular value of V_{BB} is called the characteristics of UJT

→ For a particular fixed value of V_{BB} such characteristic is shown in the fig

→ The characteristics can be divided into three main regions which are

1) Cut-off region:- The emitter voltage V_E is less than V_p and the p-n junction is reverse biased. A small amount of reverse saturation current I_{EO} flows through the device, which is negligibly small of the order of μA.

This condition remains till the peak point.

Negative resistance region:- When the emitter voltage V_E becomes equal to V_p the p-n junction becomes forward biased and I_E starts flowing. The voltage across the device decreases in this region, though the current through the device increases. Hence the region is called negative resistance region. This decreases the resistance R_{B1}. This region is stable and used in many applications. This region continues till valley point.

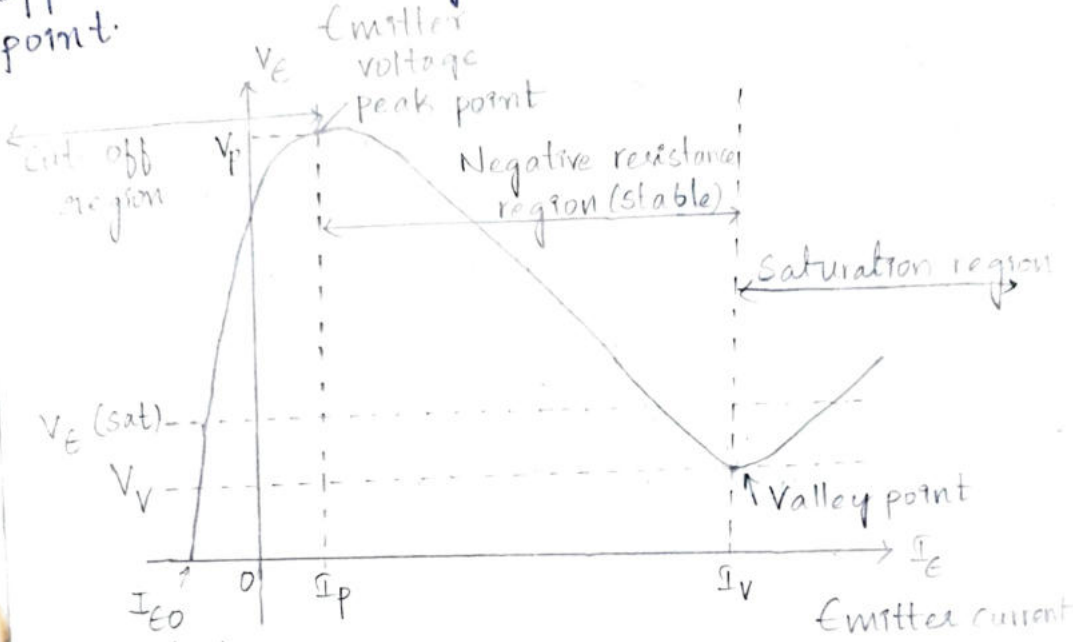


Fig: UJT characteristics

3) Satuaation Region:-

Increase in I_E further valley point current I_V drives the device in the saturation region. The voltage corresponding to valley point, denoted as V_V. In this region, further decrease in voltage does not take place. The characteristics is similar to that of a semiconductor diode, in this region

→ The active region i.e negative resistance region, the holes which are large in number on p-side, get injected into n-side. This causes increases in free electrons in the n-type slab.

This increases the conductivity i.e decreases the resistivity. Hence the resistance R_{B1} decreases in the region.

→ As the V_{BB} increases, the potential Vp corresponding to peak point will increase.

→ The typical UJT emitter characteristics for $I_{B2}=0$; $V_{BB}=20V$ and $V_{BB}=5V$ are shown in the fig.

Applications of UJT:-

The various applications of UJT are:

→ Triggering of other devices like SCR
→ In a sawtooth waveform generator
→ In a relaxation oscillator
→ In timing circuits
→ In automobile Ignition circuits.

$b = 8.786 \times 10^{-8}$ cm

FIELD EFFECT TRANSISTOR (FET):

Introduction:-

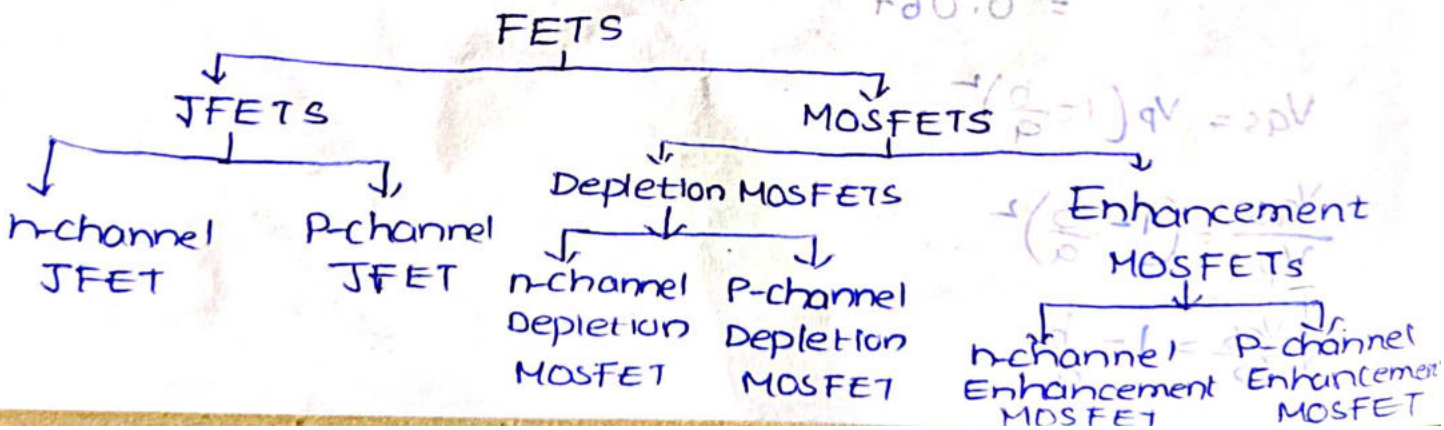
The FET stands for field effect Transistor. It is a three-terminal solid state semiconductor device in which output current is controlled by an applied electri field. It is also called a unipolar transistor because in it the current is carried by only one type of carri either electrons or holes, specially the majority carri The three terminals of a FET named as Drain (D source (S) and gate (G).

The FET's are broadly classified into two categorie

i) Junction field Effect Transistor (JFET) and

ii) Metal Oxide Semiconductor field Effect Transistor (MOSFET). It is also called Insulated Gate field Effect Transistor (IGFET).

The FET's are categorised as:



Junction Field Effect Transistor (JFET)

(A) Symbols and Terminals:

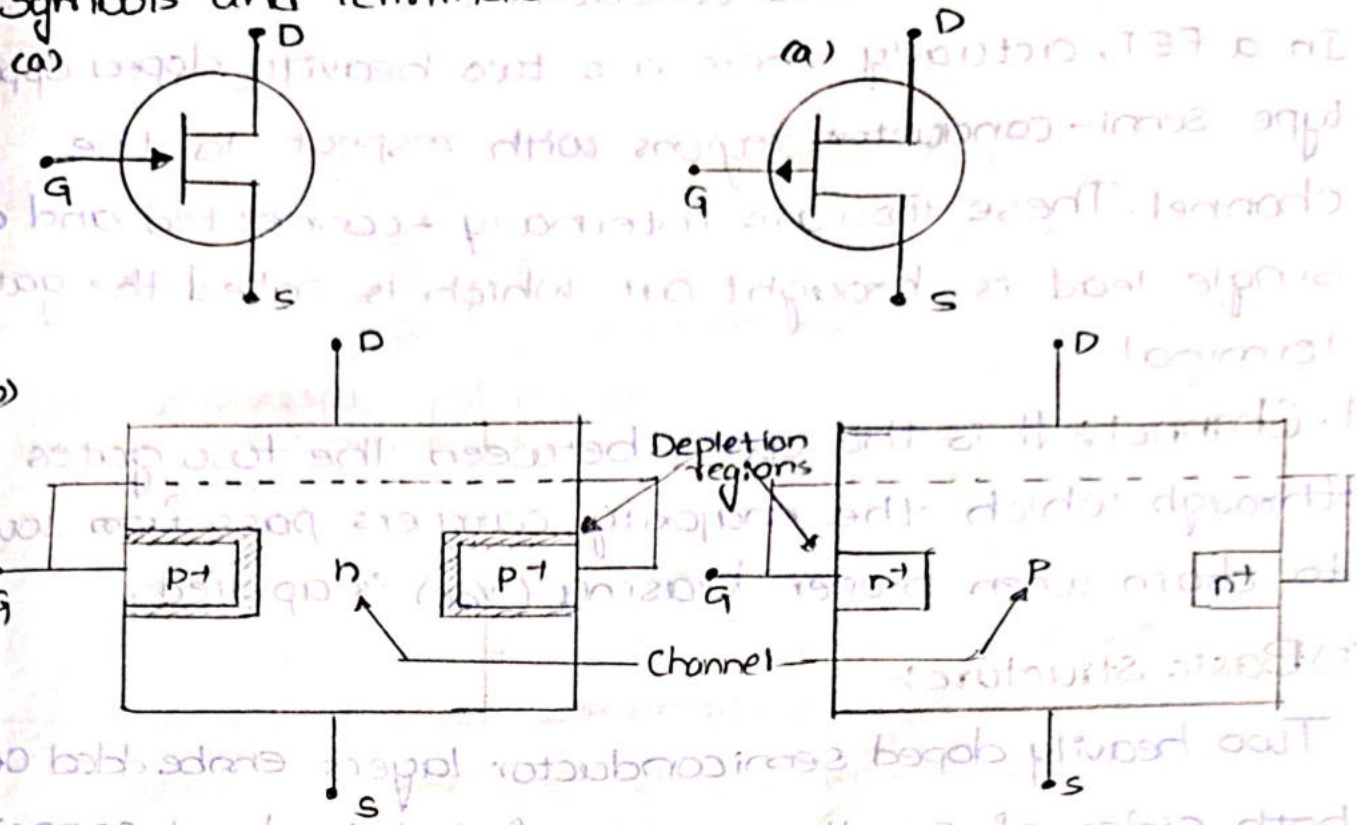


Fig: n-channel JFET
(a) Schematic symbol
(b) Structure

Fig: p-channel JFET
a) Schematic symbol
b) Structure

The terminals of an FET, i.e., source, drain and gate, corresponds to the emitter, collector and base in a BJT as follows:

1. Source :- This is the terminal where the majority charge carriers enter the channel bar to provide current through the channel. The source corresponds to the emitter of BJT. Source current is I_S.

2. Drain :- This is the terminal where the majority charge carriers leaves the channel bar. The drain corresponds to the collector of BJT. The drain current is I_D.

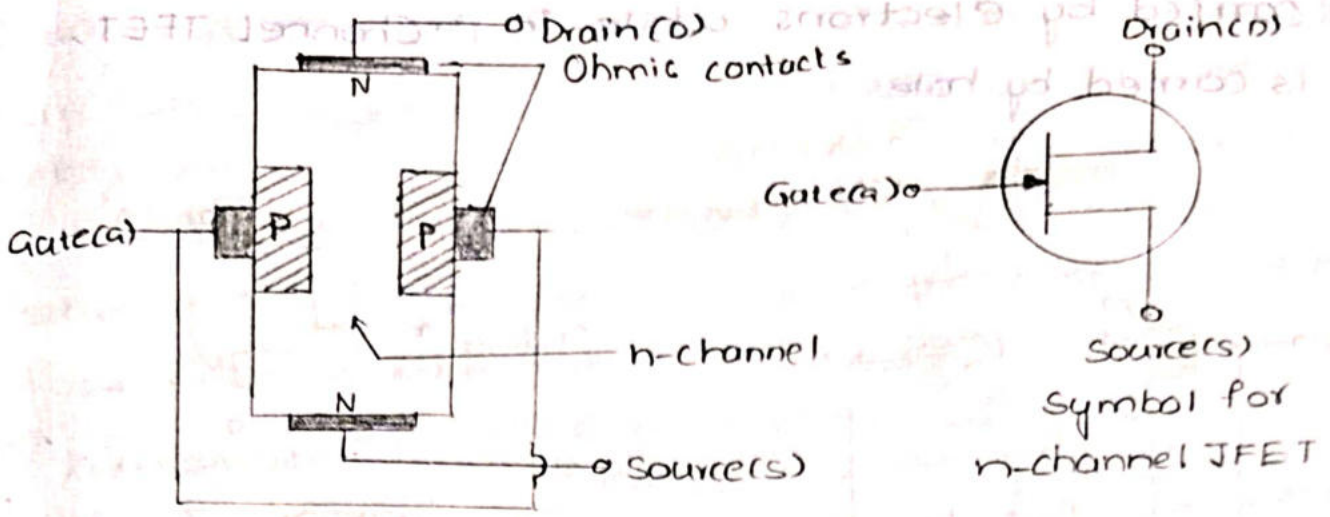
3. Gate :- This terminal corresponds to the base. terminal controls the conductance of the channe In a FET, actually there are two heavily doped opp type semi-conductor regions with respect to the channel. These two are internally-connected and single lead is brought out which is called the gat terminal.

4. Channel: It is the space between the two gates through which the majority carriers pass from sour to drain when proper biasing (V_{DS}) is applied.

(B) Basic Structure:-

Two heavily doped semiconductor layers embedded on both sides of small segment of lightly doped opposite semiconductor on its middle part such that two P-n junctions are formed. The area between the two opposite type semi-conductors is reffered to as chann The top of the channel is connected through an ohmi contact to a terminal called Drain 'D' while the lower end of the channel is connected through an ohmic contact to a terminal called source 'S'. The two opposite layers are internally connected and a single lead is brought out which is called the gate terminal.

Construction of n-channel JFET:



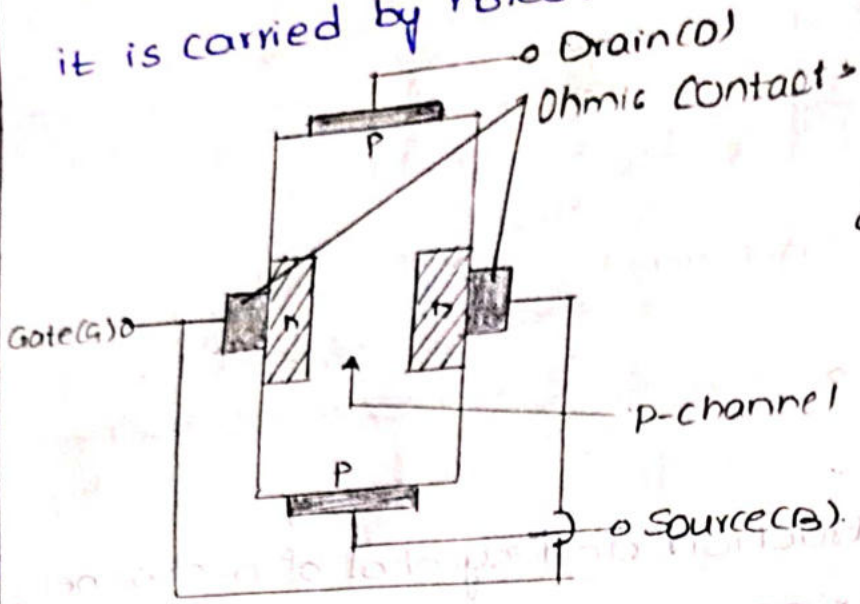
The figure shows construction and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and its two ends, two ohmic contacts are made which is the drain and source terminals of FET. Heavily doped electrodes of P type material from P-n junctions on each side of the bar. The thin region between the two P gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.

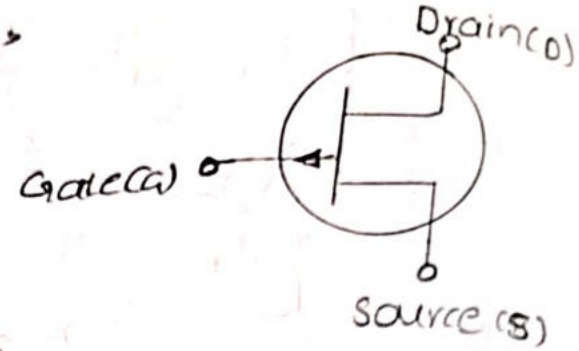
The electrons enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electronics of P-type material are called gates. These electrodes are connected together and only one terminal is taken out, which is called gate, as shown in figure.

Construction of P-channel JFET:

The device could be made of P type bar with two n type gates as shown in the figure. This will be P-channel JFET. The principle of working of n-channel JFET and P-channel JFET are similar. The only

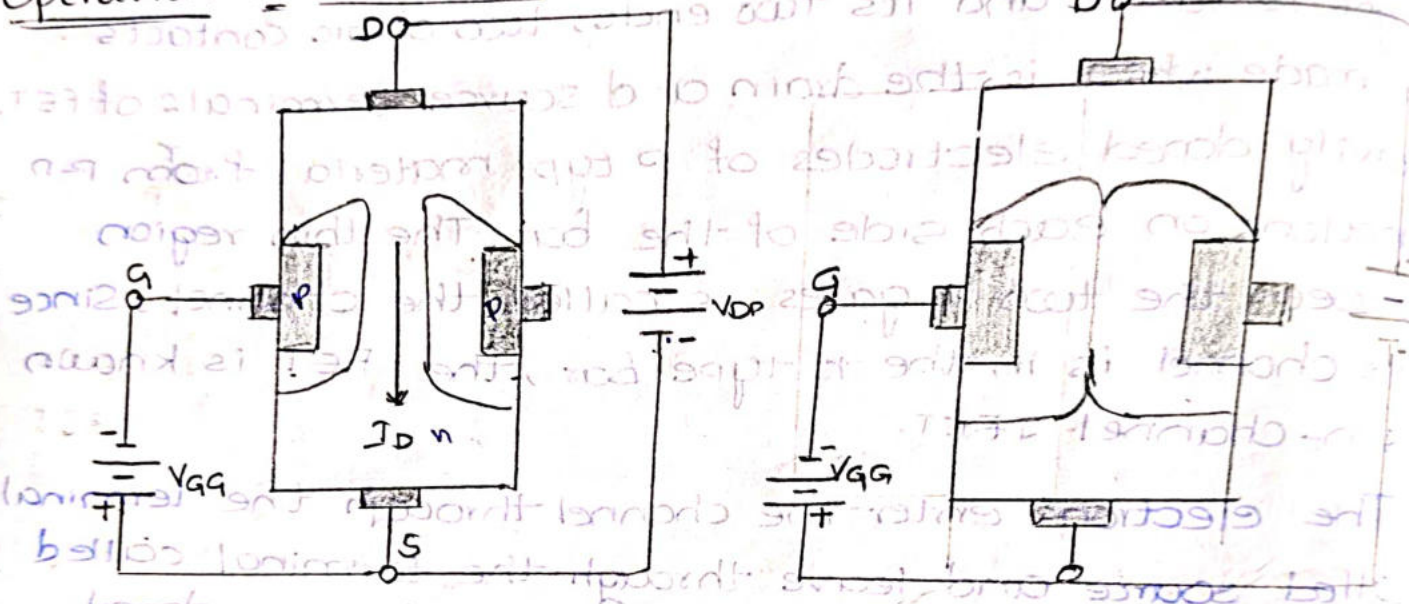
difference being
is carried by electrons while
it is carried by holes.





Symbol for p-channel JFE

Operation of n-channel JFET:-



(a) V_{GS} is less (b) V_{GS} is more

Fig: Operation of n-channel JFET

→ The n-channel JFET is biased as shown in fig. the supply voltage given to the drain and source is called V_{DD} and the one that is applied between gate and source is called as V_{GG}. When no voltage is applied between drain and source or between gate and source, the channel width remains the same as there is no change in the depletion region width.

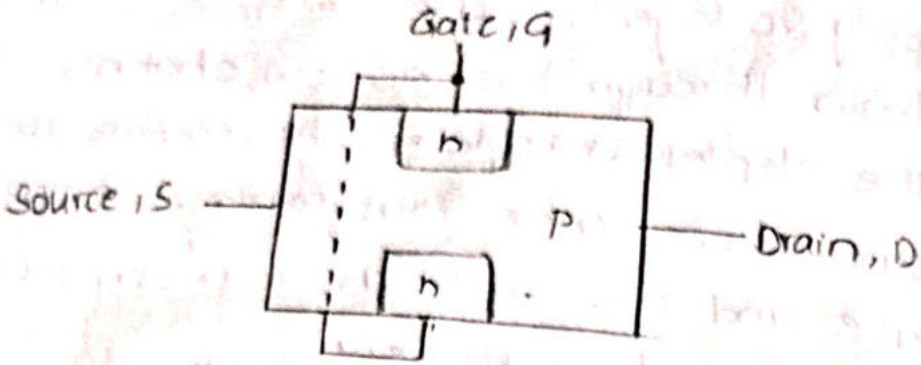
When a voltage is applied between the drain and source with a supply voltage V_{DD}, the electrons tend to flow from source to drain through the narrow channel that exists between the depletion regions. This causes drain current I_D to peak when no external voltage is applied between the gate and the source as it is called as I_{DSS}. This is illustrated in figure (a)

Keeping the drain-to-source voltage V_{DS} at zero and V_{GS} decreasing it from zero, the reverse bias across the gate source junction is increased. Hence, the thickness of the depletion region increases. The voltage drop in the channel is greater at the source than at the drain.

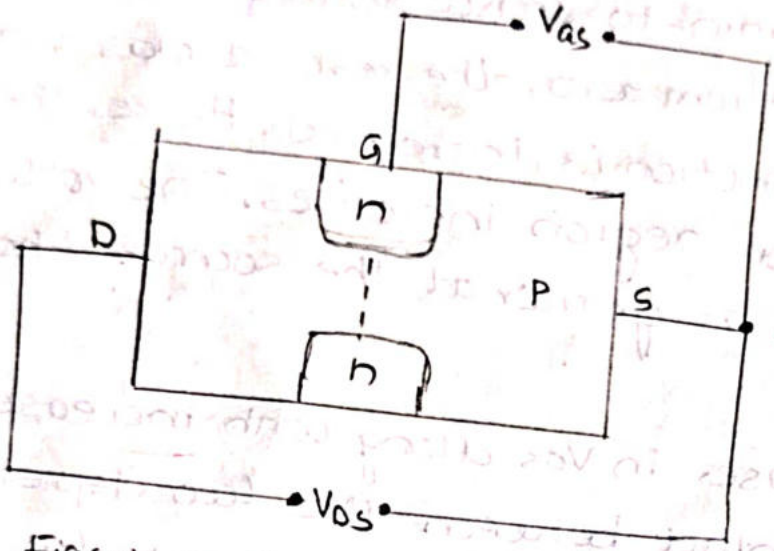
Further, increases in V_{GS} along with increased reverse bias led to contact between the two depletion regions. In this state, the channel is said to be cutoff, and the drain current is reduced to zero. The gate to source voltage V_{GS} at which the drain current is zero is known as pinch-off voltage and is denoted by V_P or $V_{GS(off)}$. This is illustrated in fig (b).

The value of pinch-off voltage is negative for n-channel JFETs. It depends on the doping of the regions and the width of the original channel. The operation of a p-channel JFET is similar to that of an n-channel JFET except that the current carriers are holes, and the polarities of the supply voltage are reversed.

Operation of P-channel JFET:-



Fig(a): Layered structured of P-channel JFET



Fig(b): P-channel JFET in a biased state

Fig1 shows the layered structure of a P-channel JFET, and fig2 shows P-channel JFET in a biased state. The P-channel JFET exhibits a mode of operation that is similar to that of its counterpart, the n-channel JFET, except for a few differences.

In case of a P-channel JFET, the major portion of the device is made of P-type, into which are embedded the two small n-type regions. Thus, it has an n-type gate terminal and a P-type source and drain, causing the channel to be of the P-type, where the holes will be the majority charge carriers. Next, the direction of the arrow in its circuit symbol is pointing outward unlike in case of n-channel JFETs.

Similar to the case of n-channel JFETs, the working of these devices also depends upon the voltages applied at their terminals.

case-(i): If $V_{DS}=0$ and $V_{GS}=0$, the device will be idle with no current, i.e., $I_{DS}=0$.

case-(ii): Now consider V_{DS} to be negative while V_{GS} is 0. At this state, the current flows from the source to the drain (as per conventional direction) as the holes within the p-substrate move towards the drain while being repelled from the source. The value of this current is restricted only by the channel resistance and is seen to increase with a decrease in V_{DS} (ohmic region). However, once the Pinch-off occurs ($V_{DS}=V_P$), the current I_{DS} saturates at a particular level of I_{DSS}, during which the device acts like a constant current source.

caseciii): Next, let V_{GS} be positive while V_{DS} is negative. Here the effect exhibited is similar to that in case (ii) with the fact that the saturation occurs at a faster rate as the V_{GS} becomes more and more positive. Similar to that seen in n-channel JFETs, even here the current ceases to flow as the value of V_{DS} becomes equal to V_P, turning the device into an off state.

Clamping Circuit Theorem:

The theorem is related to the area under output waveform in forward direction and the area under output waveform in reverse direction under steady condition.

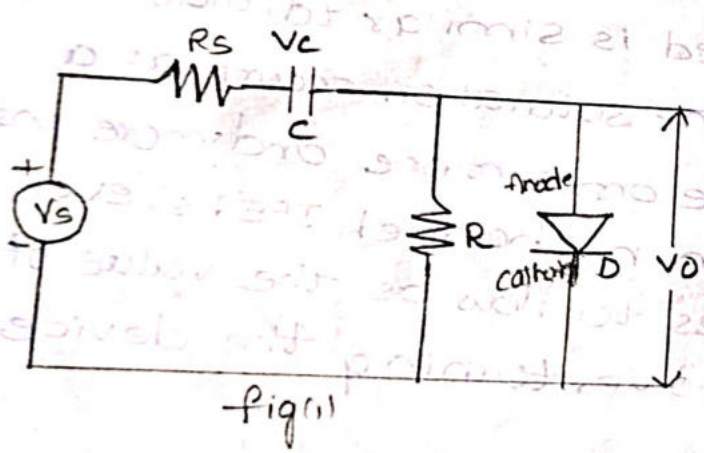
Statement: Under steady state condition for any input waveform the ratio of the area under the output curve in forward direction (when diode conducts) to the area under the output curve in reverse direction (when the diode doesn't conducts) is given by $\frac{A_f}{A_r} = \frac{R_f}{R}$

where A_f = Area under output waveform in forward direction

A_r = Area under output curve in reverse direction

R_f = Forward resistance of the diode

R = Shunt resistance (or) load resistance.



fig(1)

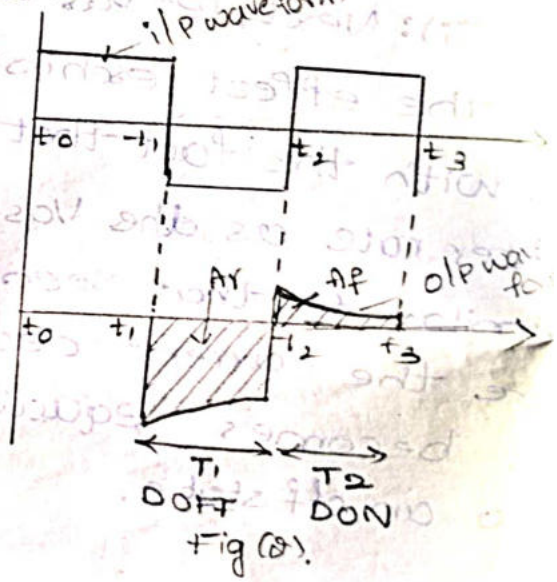


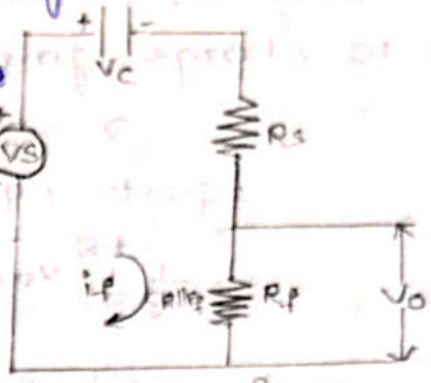
Fig (2).

Proof:

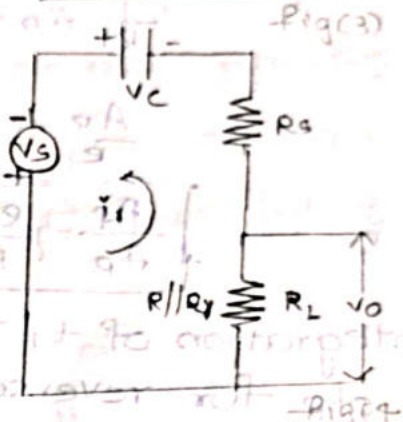
Consider the clamping circuit shown in the figure 1. The input applied is a square wave which produces the output waveform as shown in figure 2.

Let for first half cycle of input signal diode be ON, the equivalent circuit is shown in figure 3.1

During period T_1 that is form t_1 to t_2 the diode is off. Hence the capacitor discharges. Let I_1 is the discharging capacitor current.



Fig(3)



Fig(4)

→ The charge lost in the interval t_1 to t_2 is given by

$$Q_L = \int_{t_1}^{t_2} i_R \, dt$$

$$= \int_{t_1}^{t_2} \frac{V_R}{R} \, dt$$

$$\boxed{Q_L = \frac{1}{R} \int_{t_1}^{t_2} V_R \, dt} \quad \text{---(1)}$$

Where V_R = Reverse o/p voltage.

In the interval t_2 to t_3 the diode is ON the capacitor charges and regains the charge lost. Thus, if I_f is the charging current diode then charge gained

$$Q_L = \int_{t_2}^{t_3} i_f \, dt$$

$$= \int_{t_2}^{t_3} \frac{V_f}{R_f} \, dt$$

$$Q_L = \frac{1}{R_f} \int_{t_2}^{t_3} V_f \, dt \longrightarrow (2)$$

where R_f = forward resistance of diode.

Under study state conditions charge lost must be equal to charge gained that is,

$$Q_1 = Q_2$$

equate eqn ① & ②

$$\frac{1}{R}\int_{t_1}^{t_2} v_R\,dt = \frac{1}{R_f}\int_{t_2}^{t_3} v_f\,dt$$

$$\frac{1}{R}\cdot A_R = \frac{1}{R_f}\cdot A_f$$

$$\frac{A_R}{R} = \frac{A_f}{R_f}$$

$$\boxed{\frac{A_f}{A_R} = \frac{R_f}{R}}$$

But integration of t_1 to t_2 $v_R\,dt$ equal to area under o/p for reverse direction when diode is OFF. i.e equal to A_R.

$\int_{t_2}^{t_3} v_f\,dt$ area under o/p forward direction when diode is ON. i.e A_f.

UNIT-IV

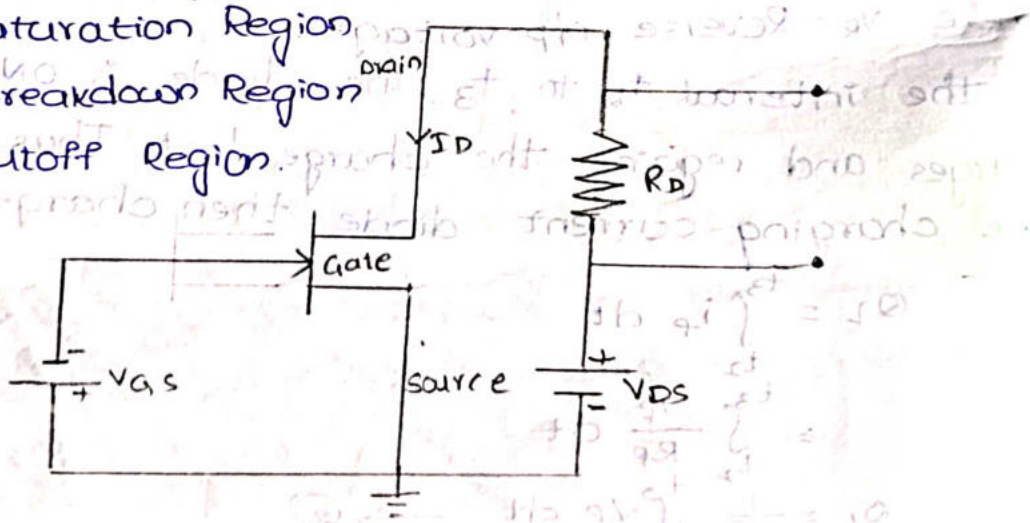
JFET as voltage variable Resistor:-

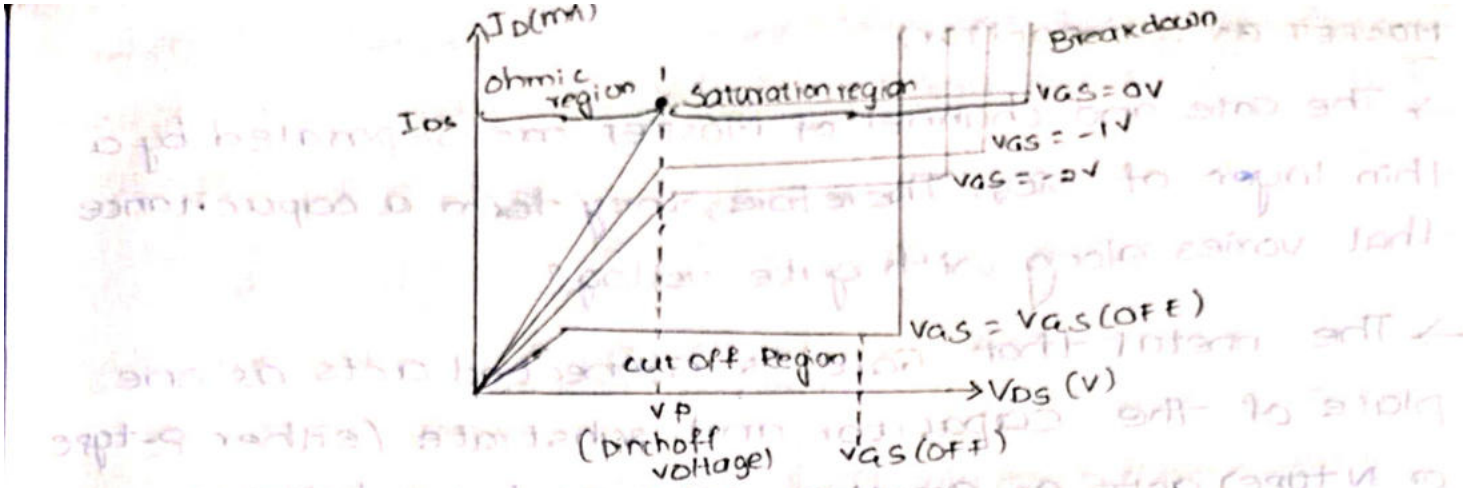
→ A JFET is a device that is usually operated in four regions i) Ohmic Region

ii) Saturation Region

iii) Breakdown Region

iv) Cutoff Region.





→ In ohmic Region JFET acts as a voltage variable Resistor.

→ In the ohmic Region, the drain-to source current (I_D) depends on the gate-source voltage (V_{GS}) & Drain to source voltage (V_{DS}).

→ For a small change in Drain to source voltage (V_{DS}), there is a change in Drain current (I_D) & FET functions as a resistor.

→ In the ohmic Region, before pinch OFF, V_{DS} is small & the drain to source Resistance r_d can be controlled by the bias voltage V_{GS}.

→ The variation of Resistance with V_{GS} can be expressed as

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

r_d = Particular drain Resistance

r_o = drain resistance at zero gate bias ($V_{GS} = 0$)

V_{GS} = Gate to source voltage.

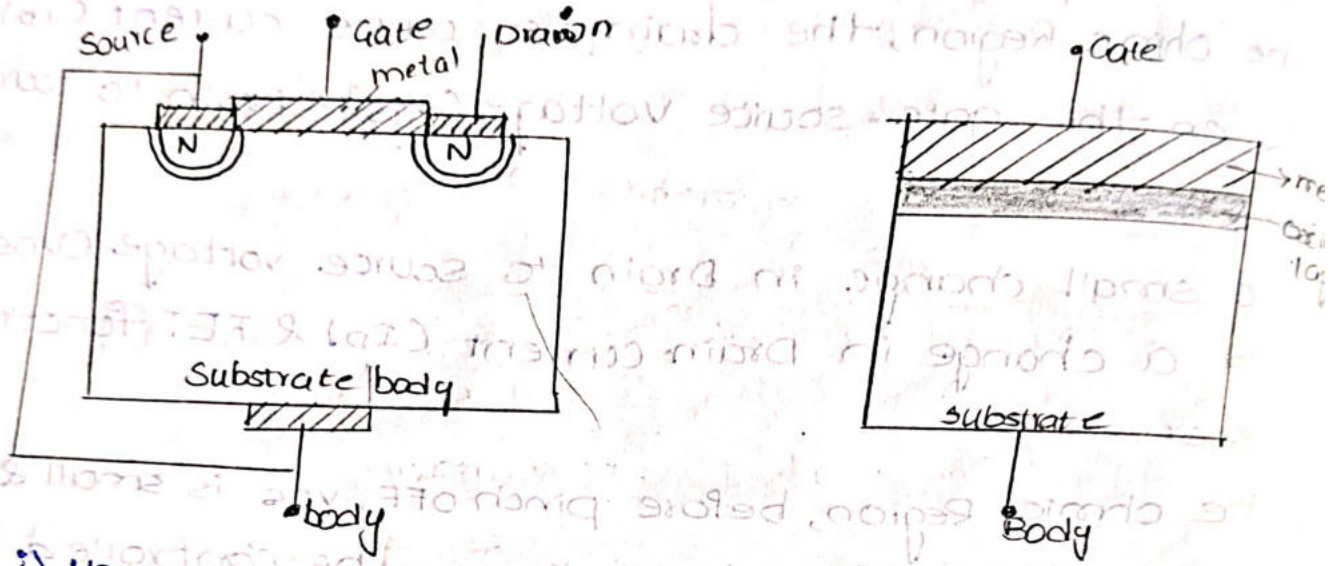
$-V_P$ = Pinch off voltage

→ Thus, Small signal FET drain resistance r_d varies with applied gate voltage V_{GS}.

MOSFET as a capacitor:-

→ The Gate and channel of MOSFET are separated b thin layer of SiO_2. Therefore, they form a capacit that varies along with gate voltage.

→ The metal that Gate is connected acts as on plate of the capacitor and substrate (either P or N type) acts as another plate and SiO_2 between capacitor plates acts as a dielectric constant.

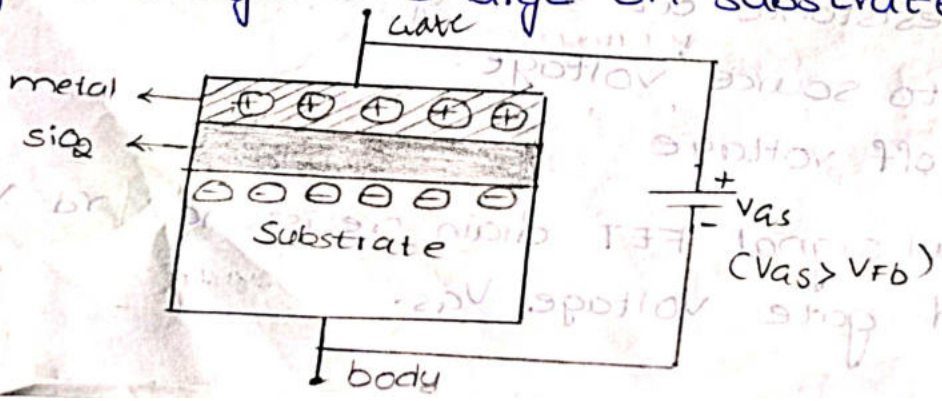


i) MOSFET structure

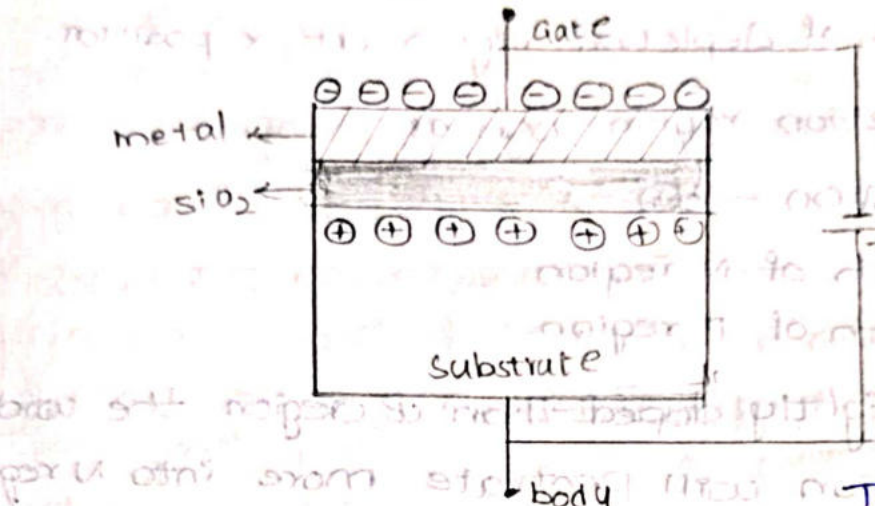
ii) MOSFET capacitor structure.

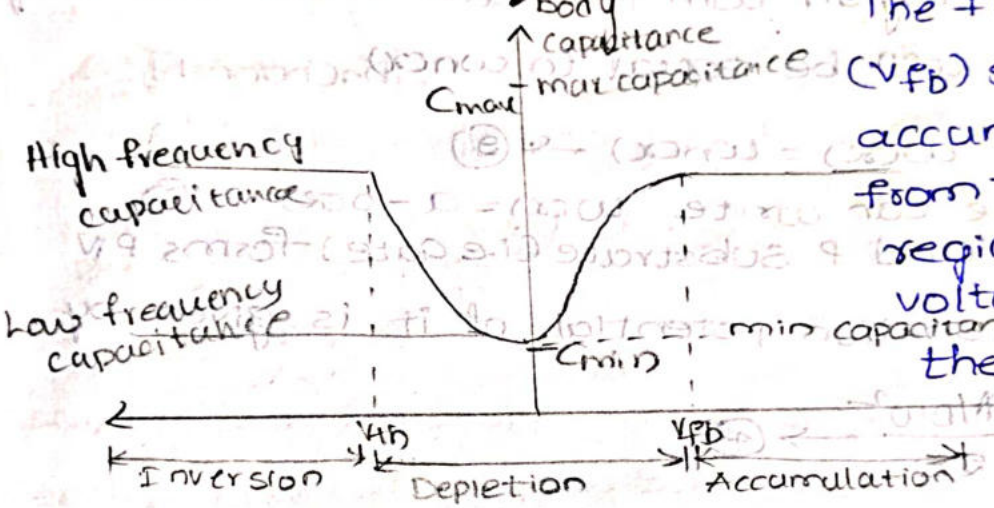
→ The capacitance of the mos capacitor depends upon the gate terminal voltage (i.e., +ve gate voltage).

→ When the applied voltage greater than the flat band voltage, the positive charge is accumulate on metal gate & negative charge on substrate



→ When the applied gate voltage is lower than the flat band voltage, then negative charge is accumulate on metal gate & positive charge on substrate.





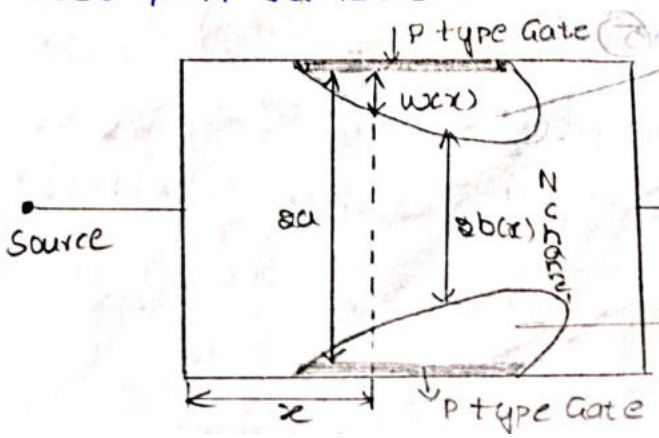
The flat band voltage (V_{FB}) separates the accumulation region from the depletion region. The threshold voltage (V_{th}) separates the depletion region from the inversion region.

Fig: Capacitance versus Gate voltage of a MOS capacitor.

Unit-IV

Pinch off voltage (V_P) of JFET:

→ In N-channel JFET N type channel is sandwiched between two heavily doped P type substrate and create two p-n junctions.



* Detail structure of n-chan

→ In the above figure.

2a = Maximum available channel width

2b(x) = Effective channel width

W(x) = The width of depletion region at x position

We can write depletion region W(x) as

$$W(x) = W_n(x) + W_p(x) \longrightarrow (1)$$

Where $W_n(x)$ = width of N region

$W_p(x)$ = width of P region

→ As n region is lightly doped than P region the w of the depletion region will pentrate more into N r So that W(x) will be equal to $W_n(x)$

$$W(x) = W_n(x) \longrightarrow (2)$$

From figure we can write $W(x) = a - b(x) \longrightarrow (3)$

→ As channel and P substrate (i.e gate) forms PN Junction the Junction potential of it is given by

$$V_j = \frac{q N_D W^2}{2\varepsilon} \longrightarrow (4)$$

$$W^2 = \frac{2\varepsilon V_j}{q N_D} \longrightarrow (5)$$

The Junction potential $V_j = V_o - V_d \longrightarrow (6)$

Where V_o = contact potential

V_d = Reverse potential applied

Substitue eqn (6) in eqn (5)

$$W^2 = \frac{2\varepsilon (V_o - V_d)}{q N_D}$$

$$W = \sqrt{\frac{2\varepsilon (V_o - V_d)}{q N_D}}$$

W = width of the depletion Region at position 'x'. So we can write W = W(x).

So above equation will become

$$W(x) = \sqrt{\frac{2\varepsilon(V_0 - V_d)}{qN_D}}$$

V_d = reverse gate voltage of PN junction at $x = V(x)$. Then, above eqn becomes

$$W(x) = a - b(x) = \sqrt{\frac{2\varepsilon(V_0 - V(x))}{qN_D}} \quad \text{—— (7)} \quad \left[\because \text{from eqn (3)}\ W(x) = a - b(x)\right]$$

Where ε = Permitivity of channel

q = charge of the electron

V_0 = Junction contact potential

$V(x)$ = Applied reverse voltage across depletion region at 'x'.

$a - b(x)$ = Penetration of depletion region into channel at 'x'.

Assume that Pinchoff occurs and when pinchoff occurs effective channel width $b(x)$ will be zero and $V(x) = V_P$

Now equation (7) becomes

$$a = \sqrt{\frac{2\varepsilon(V_0 - V_P)}{qN_D}}$$

Squaring on both sides

$$a^2 = \frac{2\varepsilon(V_0 - V_P)}{qN_D}$$

$$a^2 qN_D = 2\varepsilon(V_0 - V_P)$$

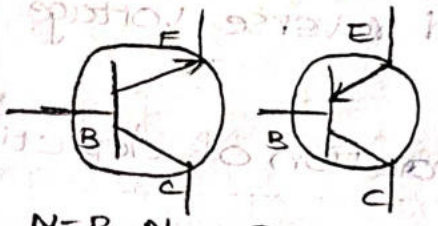
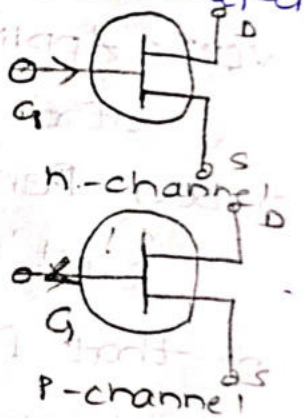
$$V_0 - V_P = \frac{qN_D a^2}{2\varepsilon}$$

$V_0 << V_P$ so we can neglect V_0. then,

$$-V_P = \frac{qN_D a^2}{2\varepsilon}$$

$$\boxed{|V_P| = \frac{qN_D a^2}{2\varepsilon}}$$

Comparison of BJT and FET:

S.No	Parameter	BJT	FET
1.	control element	current controlled device i/p current I_B control o/p current I_C	voltage control device i/p volta V_{GS} controls dra current I_D
2.	Device type	current flows due to both majority and minority carriers hence bipolar device	current flows due to majority carriers and he unipolar device
3.	Types	NPN and PNP	n-Channel & p-chan
4.	Symbols		
5.	configurations	CB, CE, CC	CD, CS, CG
6.	Input resistance	less	High
7.	Size	Bigger than JFET	Smaller in construct than BJT, thus making them useful in integrated circuits
8.	sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage
9.	Thermal stability	less	more

10.	Thermal runaway	Exists in BJT, because of cumulative effect of increase in I_C with temperature resulting increasing temperature in the device	Does not in JFET, because drain resistance R_D increases with temperature which reduces I_D, reducing the I_D and hence the temperature of the device.
11.	Relation blw i/p & o/p	linear	non-linear
12.	Ratio of o/p to i/p	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$g_m = \frac{\Delta I_d}{\Delta V_{GS}}$
13.	Thermal noise	more in BJT, as more charge carriers cross junction.	Much lower in JFET as very few charge carriers cross the junction.

Types of field effect transistors

Field effect transistors

- JFET (Junction field effect transistor)
  - n-channel JFET
  - P-channel JFET
- MOSFET (Metal oxide semiconductor field effect transistor)
  - D-MOSFET (Depletion)
    - n-channel
    - P-channel
  - E-MOSFET (Enhancement)
    - n channel
    - P channel

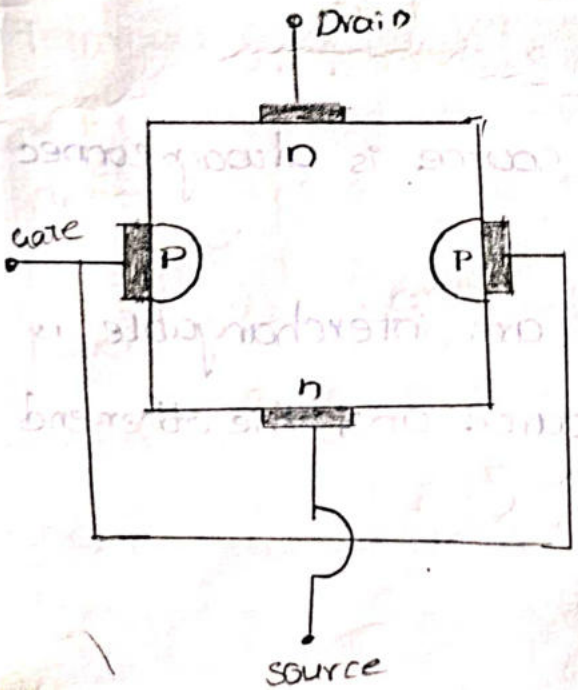
JFET construction and working of N-channel JFET

(or)

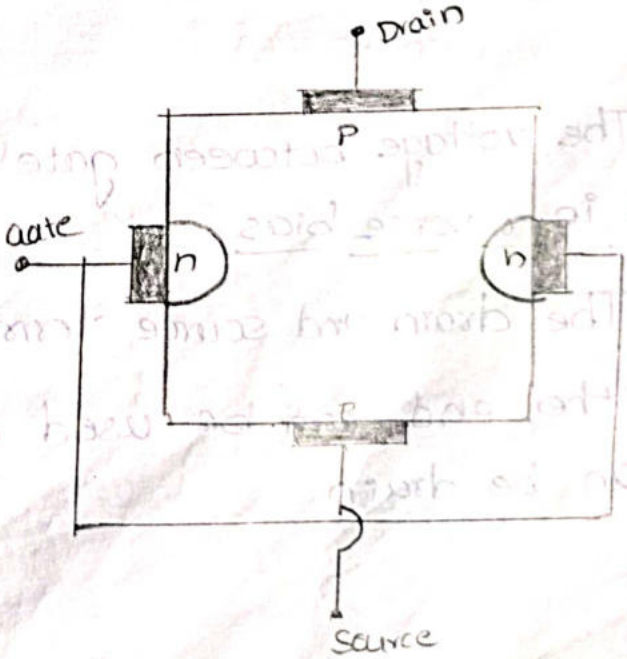
Construction and operation of JFET / construction of JFET

→ A JFET consists of P-type or n-type silicon bar containing two PN junctions at the sides and this bar forms the conduction channel for the charge carriers.

N-channel JFET



P-channel JFET



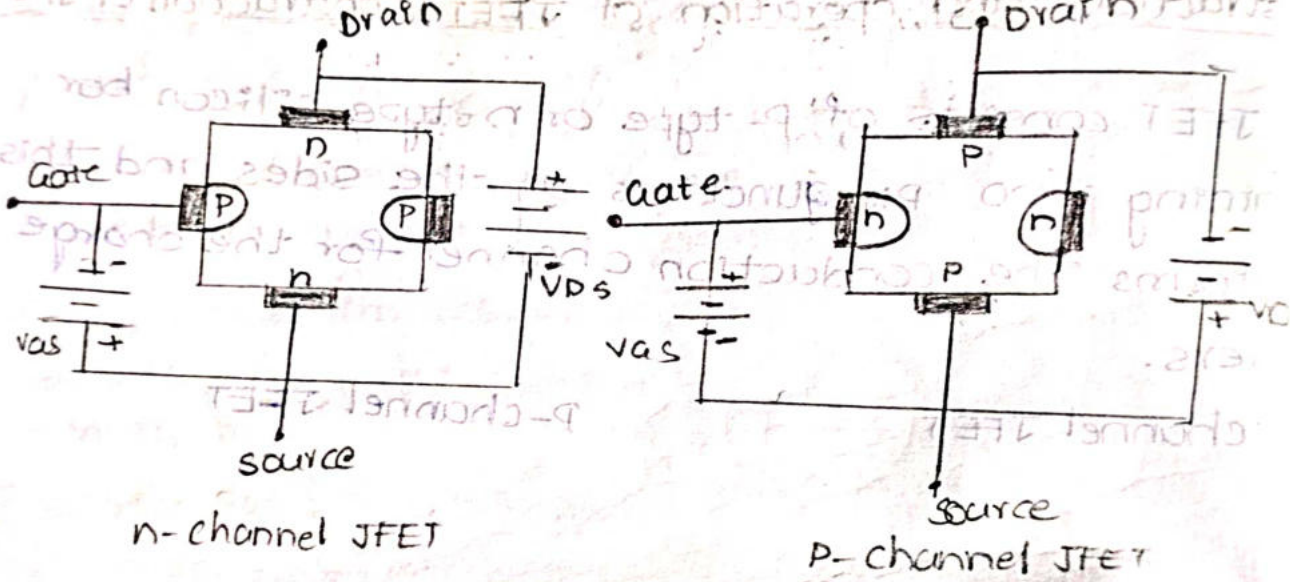
→ If the bar is of n-type it is called n-channel J
and if the bar is of p-type it is called p-channel

→ The two PN junctions form diode and are connecte
internally and a common terminal is taken out wh
is known as Gate.

→ Other terminals are taken out from the bar and a
named as source and drain.

→ JFET has 3 terminals.
Drain, Gate, source.

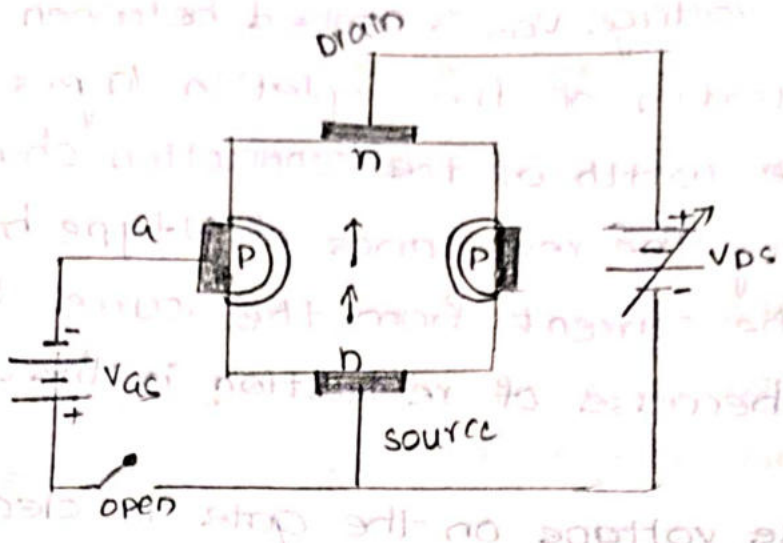
JFET polarities



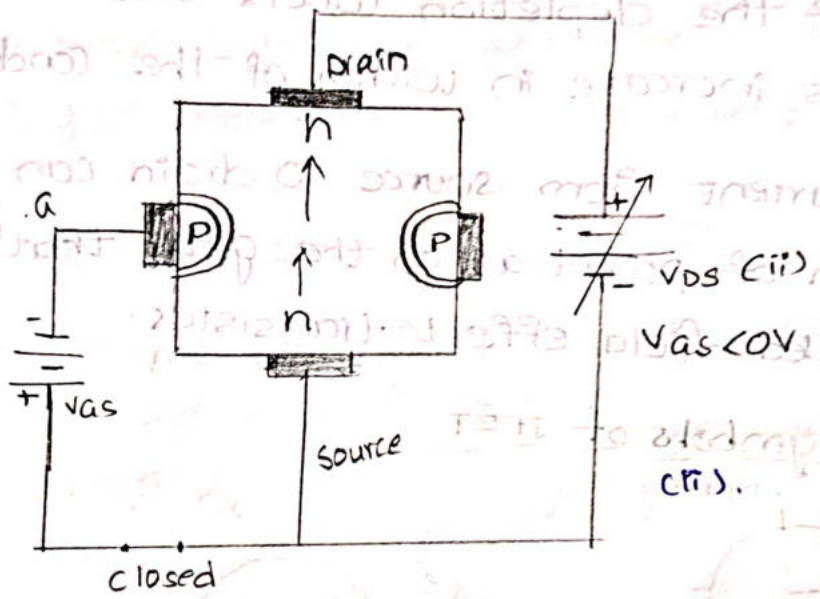
→ The voltage between gate and source is always conne
-ted in reverse bias.

→ The drain and source terminals are interchangable
either end can be used as source and the other end
can be drain.

Working principle of JFET:-



i) $V_{GS} = 0V$



(i)

→ When a voltage V_{DS} is applied between drain and source terminals and the voltage on the gate is zero ($V_{GS} = 0V$) the 2 PN junctions at the sides of the bar established depletion layers the electrons will flow from source to drain through a channel between the depletion layers.

→ The side of these layers determines the width of the channel and hence the current conduction through the bar is controlled.

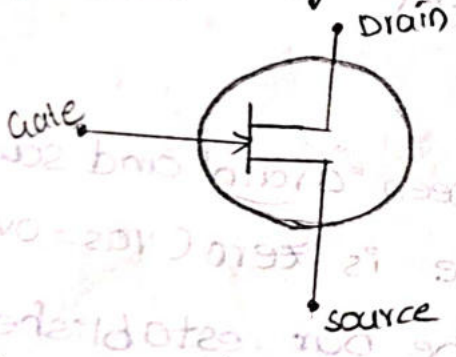
(ii)

→ When a reverse voltage V_{GS} is applied between the g and source the width of the depletion layers is inc this reduces the width of the conduction channel there by increasing the resistance of N-type bar consequently the current from the source to dra is decreases because of reduction in the channel w

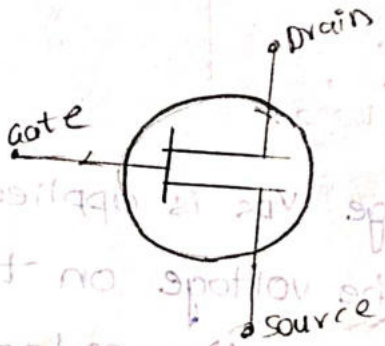
→ If the reverse voltage on the gate is decrease the width of the depletion layers also decreases hence there is increase in width of the conduction ch

→ In FET, current from source to drain can be contr by application of potential on the gate that's why th device is called field effect transistor.

Schematic symbols of JFET



fig(i): n channel JFET



fig(ii): P- channel JFET

→ If the channel is n-type the arrow on the gate points towards the channel as shown in fig(i)

→ For p-type channel the arrow on the gate points from the channel to gate as shown in fig(ii).

Merits of JFET over BJT

(or)

Difference between JFET and Bipolar transistor

→ In a JFET there is only one type of case - Holes in the p-type channel and electrons in n-type channel. Due to this reason, it is called a unipolar transistor, In ordinary transistors, both holes and e^- participate in conduction so it is called a bipolar transistor.

→ As the input circuit of the JFET is reverse biased, it offers high input impedance where as the input circuit of an ordinary transistor is forward biased and offers low input impedance.

→ In JFET, gate to source voltage controls the drain current. For this reason, JFET's are also called voltage control devices where as an ordinary transistor the base current controls the output current that's why they are called as current control device.

→ In JFET there are no junctions as in ordinary transistor the conduction is through an n-type or p-type semiconductor materials. For this reason, noise level in JFET is very small.

→ FET's have better thermal stability.

→ In integrated circuit from, FET's are to fabricate and occupy less space.

Disadvantages or limitations of JFET over BJT:

→ The main draw back of JFET's is that they have smaller gain bandwidth product when compared to BJT.

(i) Application of FET:

1) Can be used as a buffer amplifier.
2) Phase shift oscillator.
3) In volt metres.

As a buffer amplifier:

It isolates the preceding stage from the following stage because of high input impedance and low output impedance FET acts as an excellent buffer amplifier.

Phase shift oscillators:

The high input impedance of FET is especially valuable phase shift oscillators to minimize loading effect.

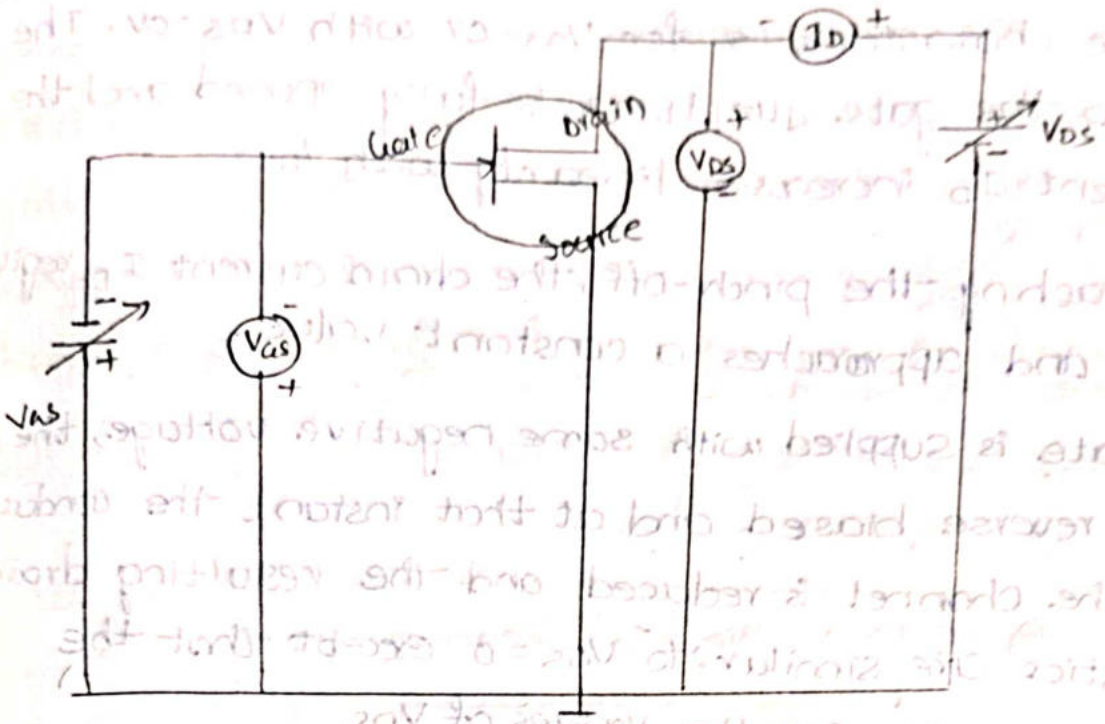
In volt meters:

The high input impedance of FET is useful in voltmeter to act as input stage.

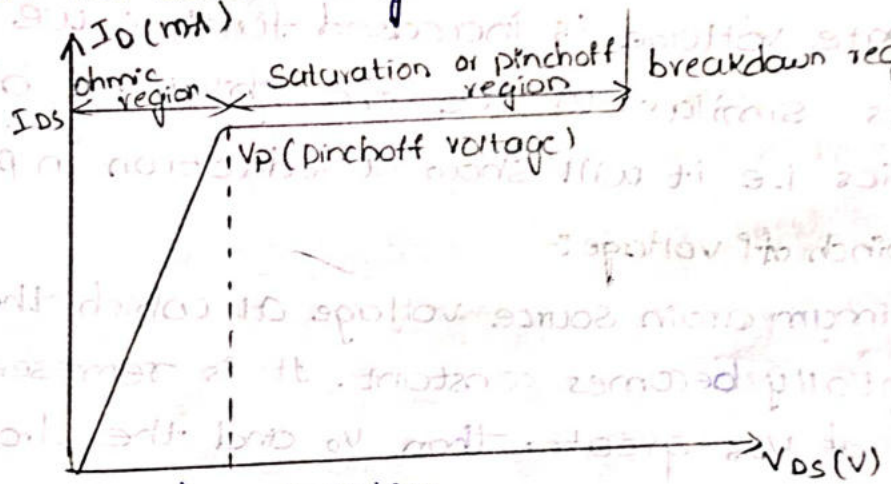
Applications of BJT:

1) used in logic circuits
2) used as an oscillator
3) used as an amplifiers
4) used as a multivibrator
5) Used as detector or demodulator
6) Also used as modulator.
7) For wave shaping it is used in clipping circuits.
8) Used in switching circuits.
9) Used in timer and time delay circuits.

Drain characteristics of JFET :



Circuit for determining drain characteristics



Drain characteristics

→ The curve between drain current (I_D) and drain source voltage (V_{DS}) of a FET at constant gate source voltage V_{GS} is called drain or output characteristics of FET.

→ Keep V_{GS} fixed at some value and change the drain source voltage in steps and notedown the corresponding drain current I_D. Plotting these values on a graph gives the o/p characteristics of FET.

→ To understand the nature of drain characteristics, let consider the characteristics for $V_{GS}=0V$ with $V_{DS}=0V$. Th channel blw the gate junctions is fully opened and th drain current I_D increases linearly with V_{DS}.

→ After reaching the pinch-off, the drain current I_D re to level off and approaches a constant value.

→ If the gate is supplied with some negative voltage, th junction is reverse biased and at that instant the cond portion of the channel is reduced and the resulting dr characteristics are similar to $V_{GS}=0$ except that the pinchoff occurs at smaller values of V_{DS}.

→ If the gate voltage is increased further, we obtain characteristics similar to the one obtained above all characteristics i.e it will show a reduction in pinchoff v

Definition of pinch off voltage:-

It is the minimum drain source voltage at which the drain current essentially becomes constant. It is represented by V_p, for values of V_{DS} greater than V_p and the drain curre is almost constant.

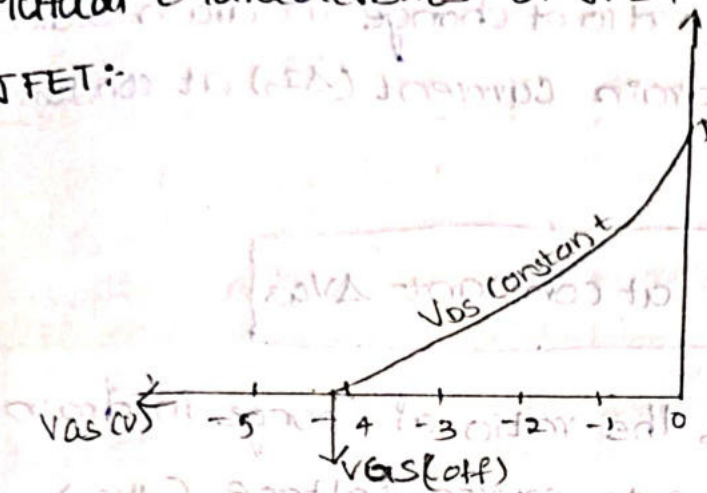
Various regions of drain characteristics:-

Ohmic region:- This part of the characteristics is linear indicating that for low values of V_{DS} current varies directly with voltage following Ohm's law.

Pinchoff region or Saturation region:- In this region JFET acts as a constant current source. It is also called as amplified region.

Breakdown region:- If V_{DS} is increased beyond its value JFET enters into breakdown region where to increases to an excessive value. This happens because the reverse based gate channel PN junction undergoes avalanche breakdown when small change in V_{DS} produces large change in I_D.

Mutual characteristics of JFET (or) Transfer characteristics of JFET:-



→ It is a plot of I_D versus V_{GS} for a constant value of V_{DS}. It is similar to the trans conductance of transistor.

→ It is seen that when $V_{GS}=0$ then I_D equal to I_{DSS} ($I_D=I_{DSS}$)

→ Gate to source cut off voltage i.e $[V_{GS(off)}]$ under trans characteristics is equal to the pinch off voltage V_P.

$$V_P = |V_{GS(off)}|$$

→ From the figure, transfer characteristics of JFET is a part of parabola then expression for drain current is given by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

I_D = drain current at given V_{GS}

I_{DSS} = Short gate drain current

V_{GS} = gate source voltage

V_{GSoff} = gate source cutoff voltage.

Parameters of JFET and relation among them.

The main parameters of JFET are:-

1) Ac drain resistance (r_d)
2) Trans conductance (g_m)
3) Amplification factor

1) Ac drain resistance:- It is the ratio of change in drain source voltage (ΔV_{DS}) to change in drain current (ΔI_D) at constant gate source voltage V_{GS}.

Ac drain resistance $\boxed{r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } \Delta V_{GS}}$

2) Trans conductance (g_m):- It is the ratio of change in drain current (ΔI_D) to change in gate source voltage (ΔV_{GS}) at constant drain source voltage (ΔV_{DS})

Trans conductance

$$\boxed{g_m | g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } \Delta V_{DS}}$$

3) Amplification factor (μ):- It is ratio of change in drain source voltage (ΔV_{DS}) to change in gate source voltage (ΔV_{GS}) at constant drain current (ΔI_D).

$$\boxed{\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } \Delta I_D}$$

Relation among JFET parameters:-

we know that $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiply the numerator and denominator of μ with ΔI_D then we get,

$$\mu = \frac{\Delta V_{DS} \times \Delta I_D}{\Delta V_{GS} \times \Delta I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

Amplification factor = AC drain resistance × trans conductance

Difference blw JFET and MOSFET:

JFET	MOSFET
1. JFET stands for Junction field effect transistor.	1. MOSFET stands for metal oxide Semiconductor field effect transistor.
2. There are two p-regions in n-channel JFET and two n-regions in p-channel JFET.	2. There is only one p-region in n-channel MOSFET & one n-region for p-channel MOSFET.
3. The channel and gate forms a pn junction.	3. The channel and gate forms a parallel plate capacitor.
4. JFETs can be operated in depletion mode.	4. MOSFETs can be operated in either enhancement mode or Depletion mode.
5. In a FET, the source to drain current is controlled by the reverse bias voltage to the gate.	5. In a MOSFET the source to drain current is controlled by electric field of capacitor formed at the gate.
6. Input impedance in the range of 100MΩ.	6. Input impedance in the range of 10,000MΩ to 10,00,000MΩ
7. Manufacturing process is simple.	7. Manufacturing process is Complex.

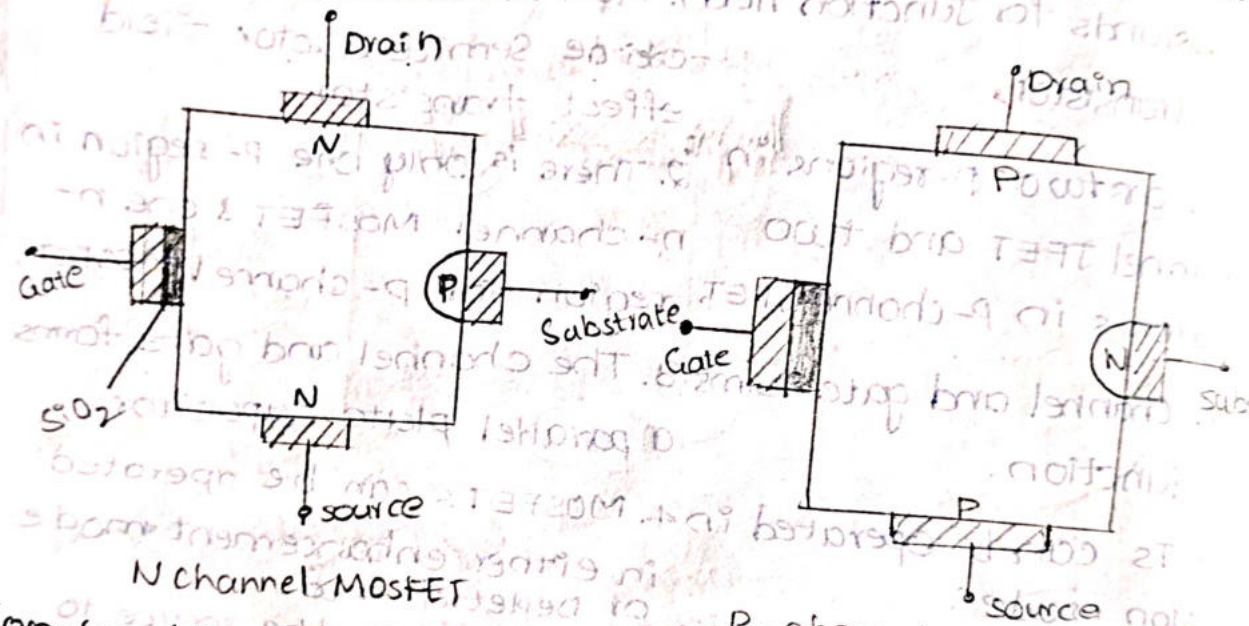
Construction and working of MOSFET :-
(N-channel & P-channel)

Construction of MOSFET:-

→ There is only single P-region in N-channel FET & one single N-region in P-channel FET called as substrate.

→ A thin layer of metal oxide (usually silicon dioxide) is deposited over the left side of the channel. A metal gate is deposited over the oxide layer. As silicon dioxide is an insulator, therefore gate is insulated from the channel, for this reason, MOSFET is sometimes called insulated gate FET (IGFET).

→ Like JFET, a MOSFET has four terminals. Source, gate & drains & substrate.



Construction and working of depletion type N-channel MOSFET

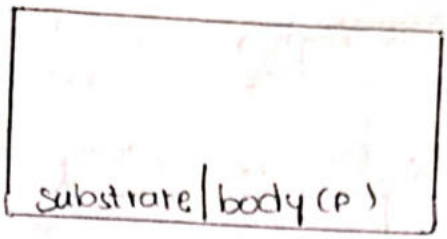
Construction of depletion type N-channel MOSFET :-

→ In depletion type MOSFET channel is present from the begining in between source and drain.

→ Depletion type N-channel MOSFET consist of four terminals 1) P substrate, 2) source, 3) Gate, 4) Drain.

i)

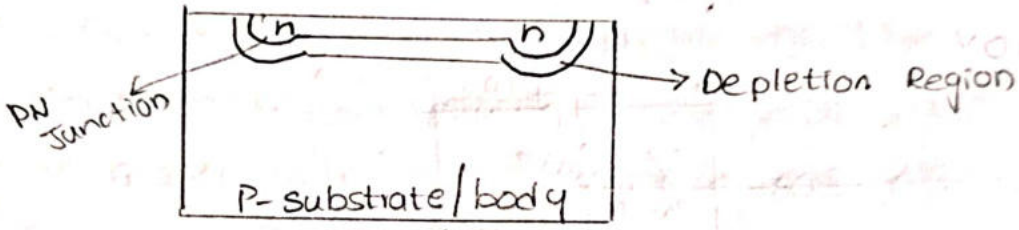
→ P-type substrate is formed by adding trivalent impurities to silicon wafer.



Formation of P-type substrate

ii)

→ Two n-type wells are induced in the p type substrate.



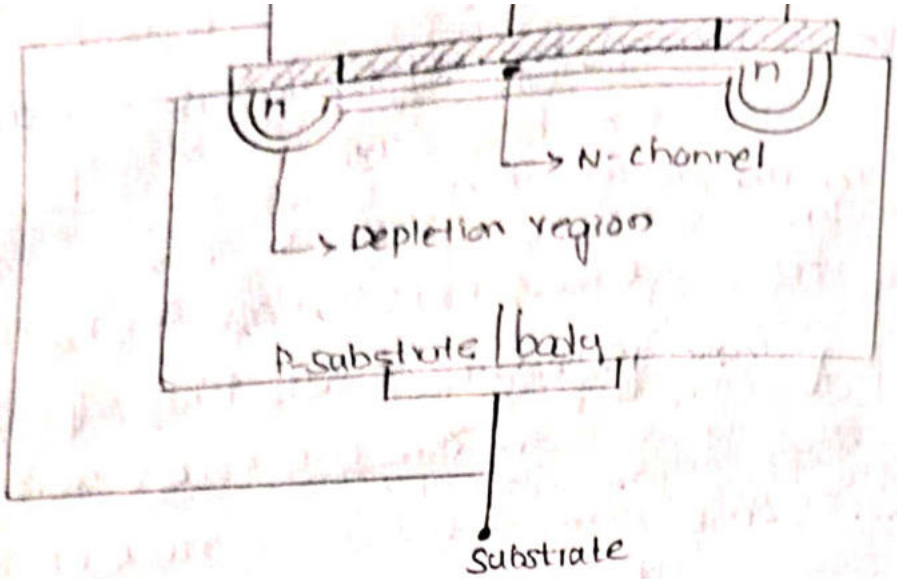
Formation of N-type wells

→ After creation of two N-type wells there is two junctions formed between two n-type materials and p-type substrate due to this two depletion region with same width will be formed.

→ One n well acts as source and other will be drain.

→ Source, drain and substrate will be taken out from the p-type substrate/body with the help of metal contact.

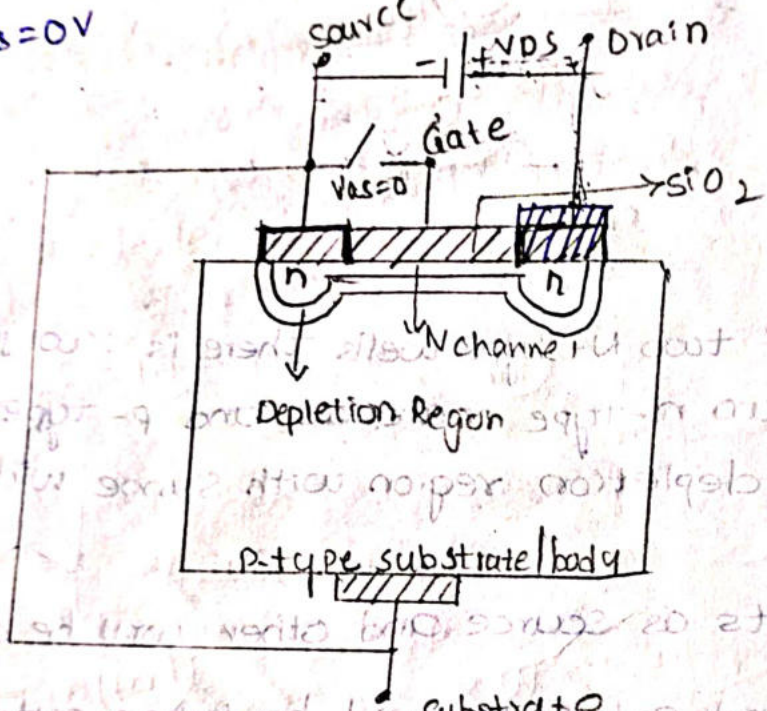
→ In MOSFET there is no direct contact in between gate terminal and channel. The gate terminal is separated from the channel by SiO_2 layer which will acts as insulator.



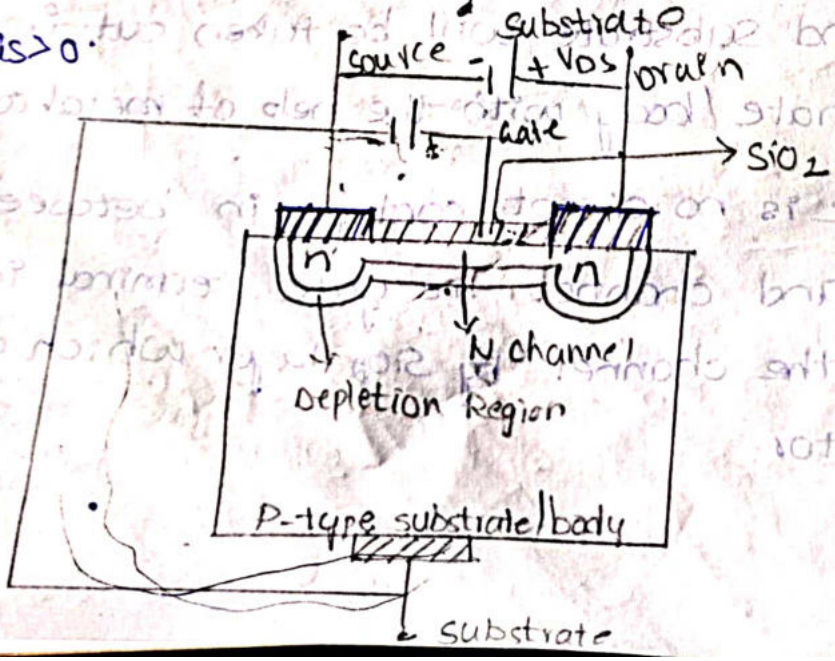
complete formation of depletion type MOSFET

Working of depletion type N-channel MOSFET :-

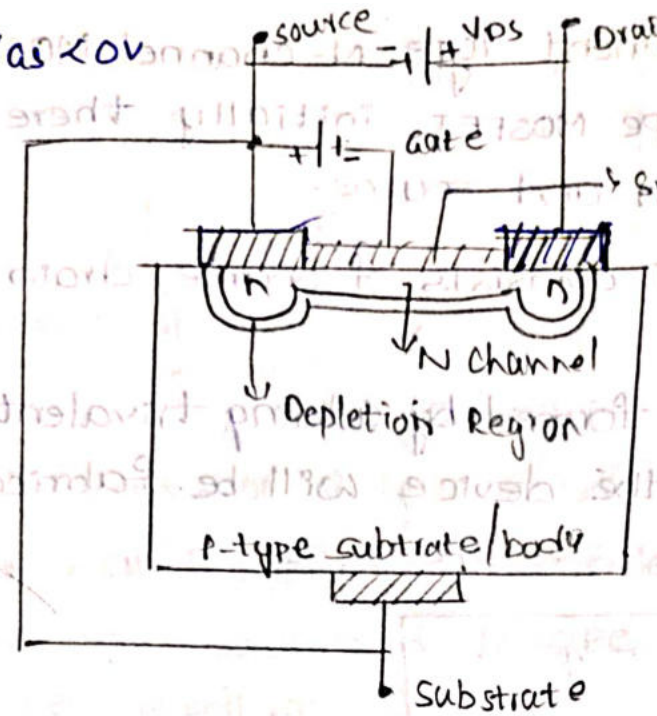
i) $V_{GS} = 0V$



ii) $V_{GS} > 0$.



iii) ∴ $V_{GS} < 0V$

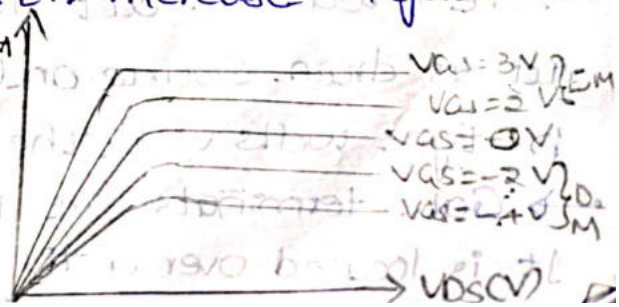


⇒ When $V_{GS} = 0V$ with the increase in V_{DS} the current I_D increases because drain is more positive so that more number of electrons attracts towards the drain terminal but after sometime pinchoff occurs and drain current will becomes constant even if we increase the V_{DS}.

⇒ When $V_{GS} > 0V$ application of positive gate voltage results induced negative polarity (charge) in the n-type channel thus the conductivity of the channel gets increased so that drain current also increases.

⇒ When $V_{GS} < 0V$.

When the gate is applied with negative voltage positive charges are induced in the n-channel and these induced positive charges makes the n-channel less conductive and the drain current decreased with increase in gate bias voltage.

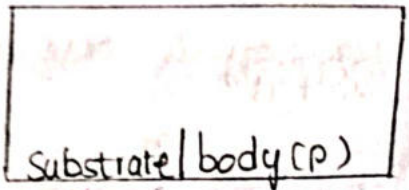


Construction of enhancement type N-channel MOSFET:

→ In enhancement type MOSFET, initially there is no channel between drain and source.

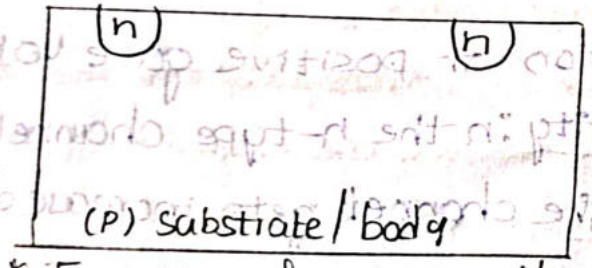
→ N-channel MOSFET consists of source, drain, gate and p type substrate.

i) P type substrate is formed by adding trivalent impu to silicon wafer and the device will be fabricated o this substrate.

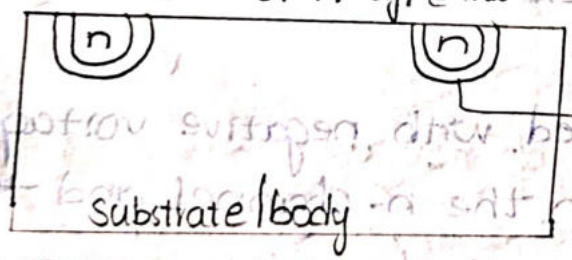


Formation of p-type substrate

ii) After these two n-type wells are created, here is junction blw two n-type materials and p-type mate and two depletion regions with same width will be formed.



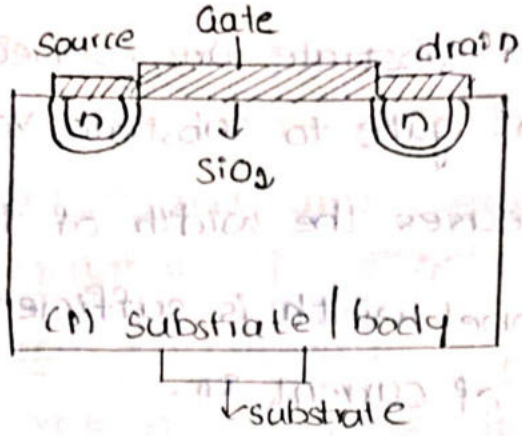
* Formation of n-type well



* Formation of depletion region

→ One n well will act as source and other n well will act as drain. Source and drain will be taken out from the n-type wells with the help of metal contact.

→ Gate terminals are not in direct contact with substra It is located over a thin layer of SiO_2 / silicon dioxides.



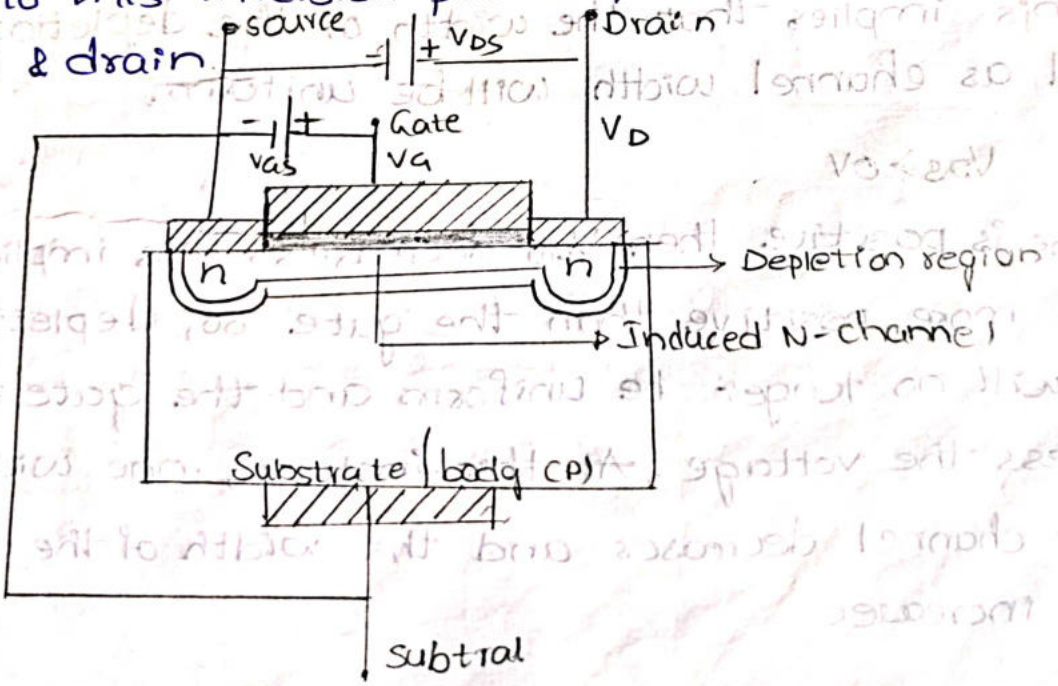
Formation of terminals

→ As SiO_2 is an insulator a parallel plate capacitor is formed between Gate and p-type substrate with SiO_2 as dielectric medium

→ If we apply normal Vas (Substrate) between Gate and p-type substrate. Positive charge will accumulate over gate plate and less number of the charges will accumulate over substrate plate.

→ If we increase Vas, more no. of -ve charges will accumulate over the substrate region & p- region near the surface will become n-region. This process is known as inversion.

→ Due to this inversion process, channel is created blw source & drain



→ In MOSFET source and substrate are connected interna
That's why we represent gate to substrate voltage at V_{GS}
→ Increase in V_{GS} increases the width of the channel
→ At $V_{GS} > V_t$ the channel width is sufficient and results in significant flow of current I_D.
→ The voltage that results in significant flow of current from source to drain is known as threshold voltag
Appling KVL to the above circuit,

$V_G - V_{GS} + V_{DS} - V_D = 0$ (consider potential differen
$V_G - V_D = V_{GS} - V_{DS}$ blw G & drain terminal
$V_{GD} = V_{GS} - V_{DS} \rightarrow (1)$ $V_G - V_D$ as V_{GD}).

Case 1 :- $V_{DS} = 0V$

Sub $V_D = 0$ in (1), we get

$$\boxed{V_{GD} = V_{GS}}$$

This means there is no potential difference blw V_{GD} or V_{GS}. This implies that the width of the depletion lay as well as channel width will be uniform.

Case 2 :- $V_{DS} > 0V$

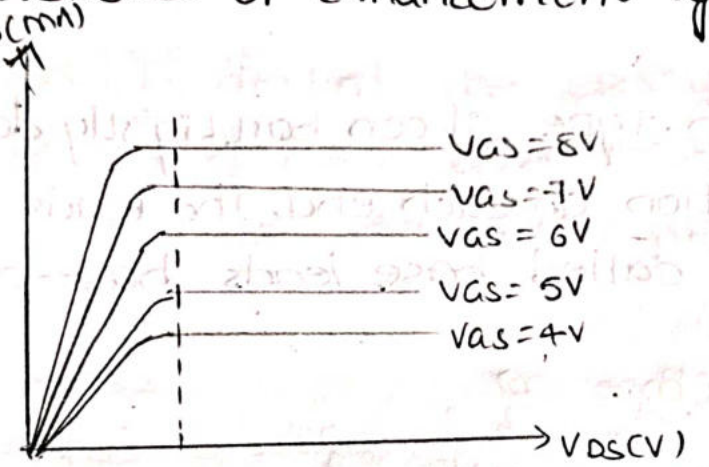
When V_{DS} is positive then V_{GD} decreases. This implies drain is more positive than the gate so, depletion region will no longer be uniform and the gate region gets less the voltage. At this instant, one width of the channel decreases and the width of the depletion region increases.

case 3: $V_{DS} = V_{GS} - V_{GD}$

. Consider V_{GD} as V_T. In this case both V_{GD} & V_{GS} are in opposite direction and can't overcome V_T. The channel becomes very narrow. If we increase V_{DS} the drain current I_D becomes almost constant. This is known as V_{DS} sat. V_{DS} sat is equal to $V_{GS} - V_T$.

$$\boxed{V_{DS} \text{ sat} = V_{GS} - V_T}$$

Drain characteristics of enhancement type N-channel MOSFET:



UJT (Unijunction Transistor):-

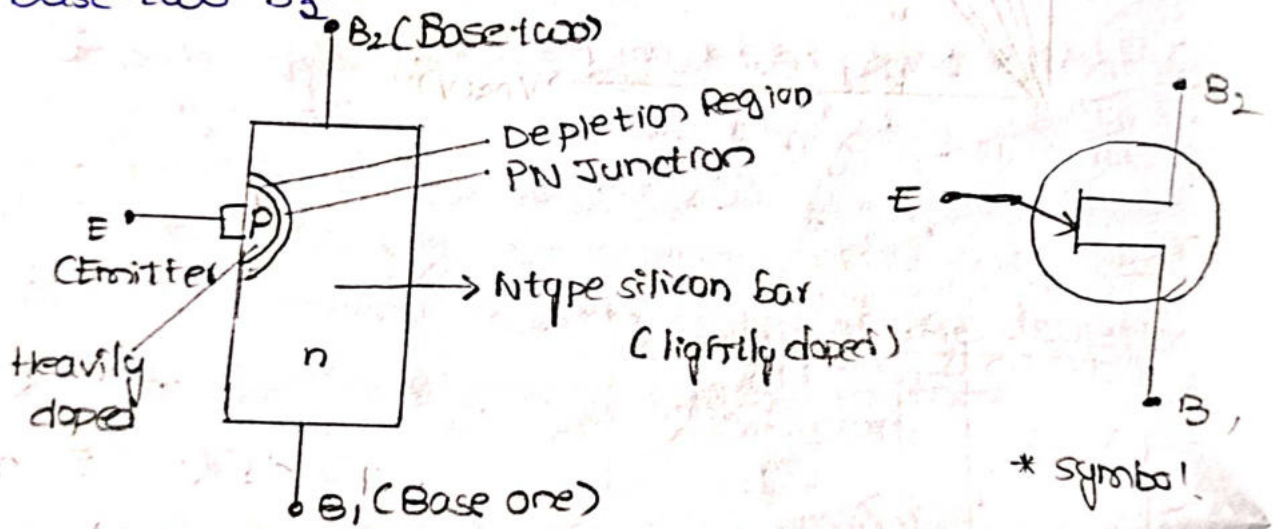
→ A Unijunction Transistor is a three terminal semico switching device.

→ This device has a unique characteristics that wh it is triggered, the emitter current increases regener until it is limited by emitter power sopply.

→ It can be used in switching, pulse generator, saw tooth generator etc.

Construction:-

→ It consists of n-type silicon bar (Lightly doped) with electrical connection on each end. The leads to these connections are called base leads base-one B_1 and base-two B_2.



→ A small piece of heavily doped P-type material is alloyed to one side of N-type bar closer to B_2 for producing single PN-Junction. The terminal taken out from P-type material is called Emitter(E).

→ In the symbol arrow indicates the direction of the conventional current.

Equivalent circuit of UJT:-

→ Equivalent circuit of UJT consists of a PN Junction diode and two resistors R_{B1} and R_{B2}

→ R_{B2} is the resistance of silicon bar between base B_2 and the emitter Junction.

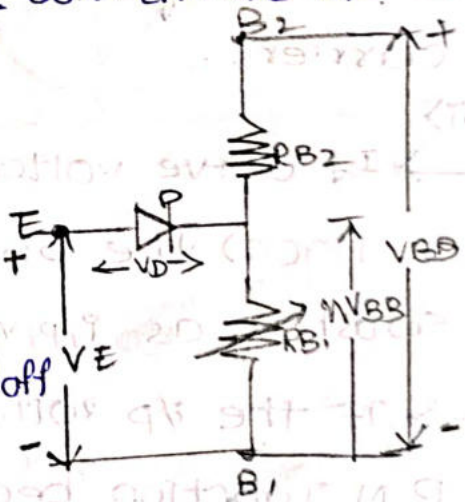
→ R_{B1} is the resistance of bar between base b_1 and emitter Junction. This resistance is variable because its value depends upon the bias voltage across the PN-Junction.

i) When no voltage applied, the resistance between base1 and base2 of the silicon bar with emitter terminal open is called the interbase resistance (R_{BB}).

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} lies b/w 4KΩ-10KΩ

ii) If a voltage V_{BB} is applied between the bases with emitter terminal open, the voltage will divide up across R_{B1} and R_{B2}.



voltage across R_{B1}, $V_1 = V_{BB} \cdot \frac{R_{B1}}{R_{B1}+R_{B2}}$

$$V_1 = \eta \cdot V_{BB}$$

where η is called the "intrinsic standoff ratio".

$$\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} = \frac{R_{B1}}{R_{BB}}$$

(or)

$$\eta = \frac{V_1}{V_{BB}}$$

The typical value of η ranges from 0.56 to 0.8.

Working principle of UJT with its equivalent circuit:

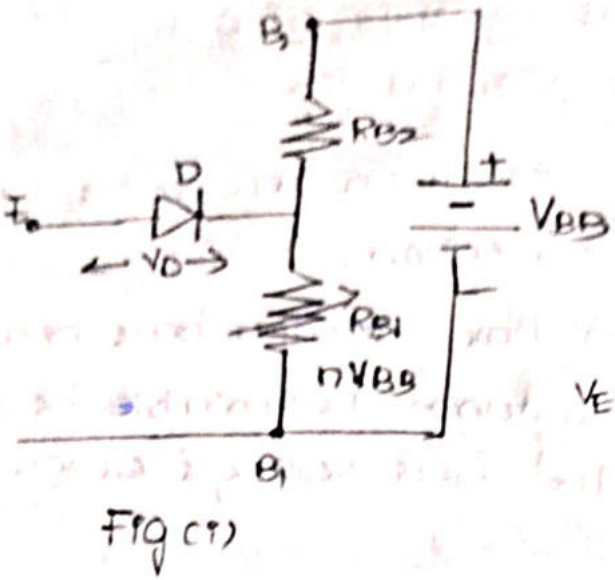


Fig (i)

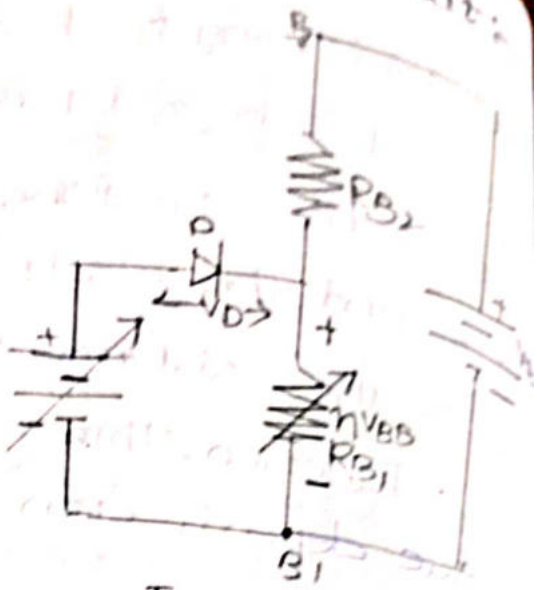


Fig (ii)

i)

→ When we apply V_{BB} between base 1 & base 2 with emitter open as shown in fig (i) the voltage grad establishes along n-type bar.

→ More than half of V_{BB} appears between emitter & B and the voltage ($V_1 = \eta V_{BB}$) between emitter & Bas establishes a reverse bias on the P-N Junction and leakage current flows due to minority carriers.

ii)

→ If a +ve voltage applied at the emitter as sho in fig (ii) the pn junction will remain reverse biase so as long as i/p voltage is less than V_1.

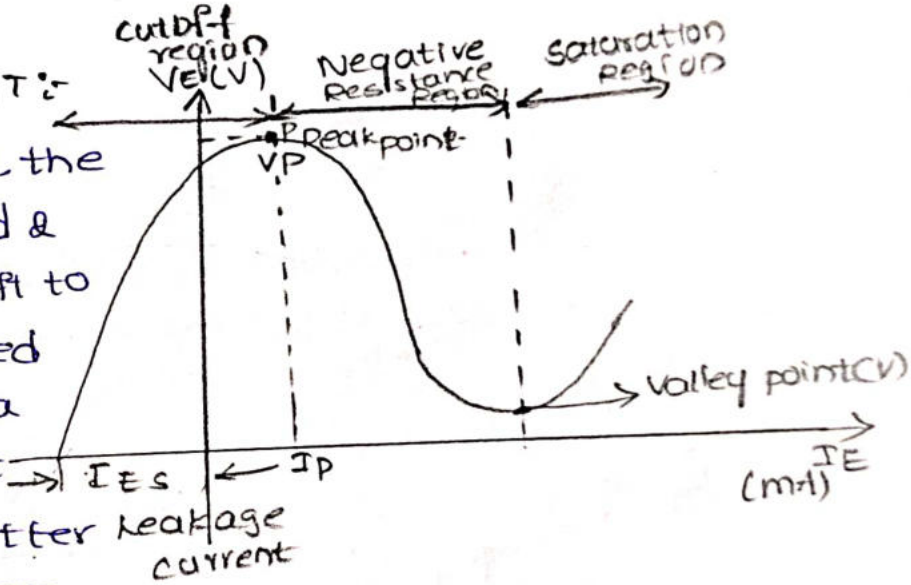
→ If the i/p voltage to the emitter exceeds V_1, the P N Junction becomes forward biased. Under these conditions the holes are injected from P-type int n-type bar. These holes are repelled by +ve B_2 terminal & they are attracted towards B_1 terminal of the bar. This accumulation of holes in the

mitter to B1 region results in the decreases of resistance in thisection of bar. The internal voltage drop from mitter to B1 is decreased and emitter current IE increases.

> As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is ~~cutoff. The device is then~~ limited by emitter power supply only. The device is now in the ON state.

:) If a -ve pulse is applied to the emitter, the PN Junction is reverse biased and the emitter current is cutoff. The device is then said to be in the OFF state.

Characteristics of UJT :-



* upto the peak point P, the diode is reverse biased & hence, the region left to the peak point is called cut-off region. But a small leakage current flows from B1 to emitter due to minority carriers.

→ At the peak point P, the diode starts conducting & holes are injected into N-layer Hence, the resistance decreases there by decreasing VE for the increase IE. so, where is a "Negative resistance region" from peak point P to valley point (V).

→ After the valley the device is driven into saturation & behaves like a conventional forward biased PN Junction diode. The region to the right of valley point

is called saturation region.

Applications of UJT:-

→ Used to generate sawtooth waveform such as relaxation oscillator.

→ Used in pulse generator.

→ Used in switching applications.

→ Used in timing circuits.

→ Phase ctrl circuits.

→ Used in sweep circuits.

→ voltage or current regulated supplies.

→ used as a trigger device for SCRs & TRIAC.

BIPOLAR JUNCTION TRANSISTOR

Introduction:-

→ The transistor was developed by Dr. shockley along with Bell Laboratories team in 1951.

→ The transistor is a main building block of all modern electronic systems.

→ It is a three terminal device whose output current, voltage and power are controlled by its input current.

→ In communication systems it is the primary component in the amplifier.

→ An amplifier is a circuit that is used to increase the stength of an ac signal.

→ Basically there are two types of transistors
- Bipolar junction transistor.
- Field effect transistor.

→ the important property of the transistor is that it can raise the strength of a weak signal. This property is called amplification.

→ A transistor consists of two P-N junctions. The junctions are formed by sandwitching either P-type or N-type semiconductor layers between a pair of opposite types which is shown below.

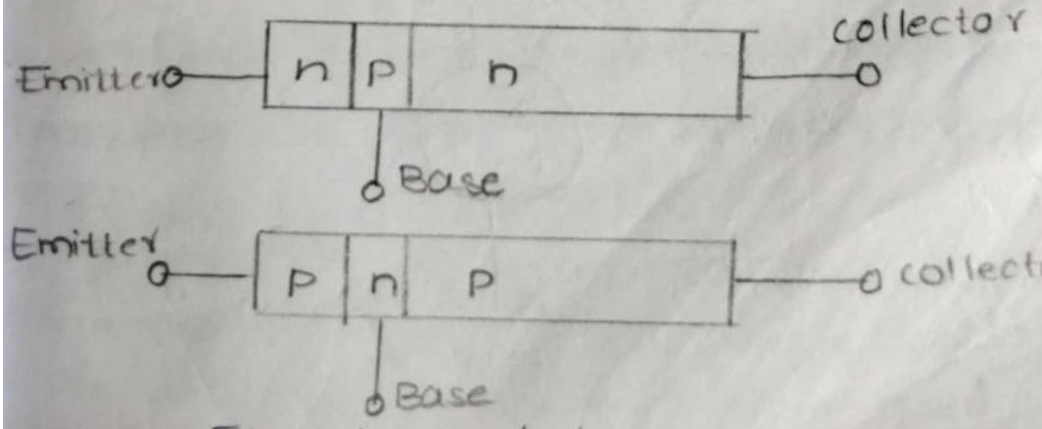


Fig: transistor

Transistor Construction:-

→ A transistor has three regions known as emitter, base and collector.

Emitter:- It is a region situated in one side of a transistor which supplies charge carriers (i.e electrons and holes) to the other two regions.

→ Emitter is heavily doped region.

Base:- It is the middle region that forms two P-N junction in the transistor.

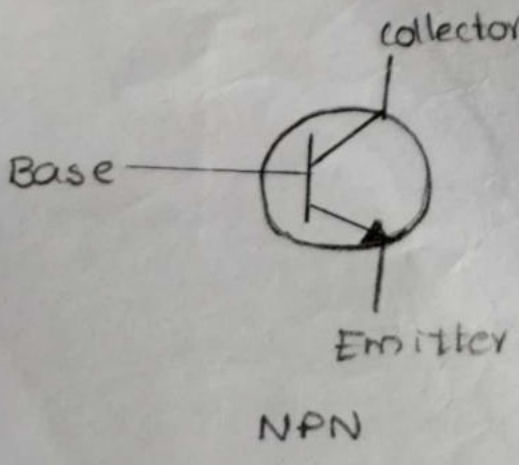
→ The base of the transistor is thin as compared to the emitter and is a lightly doped region.

Collector:- It is a region situated in the other side of a transistor (i.e opposite to the emitter) which collects the charge carriers.

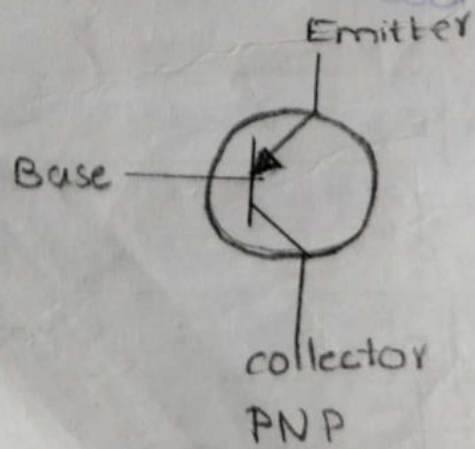
→ The collector of the transistor is always larger than the emitter and base of a transistor.

→ The doping level of the collector is intermediate between the heavy doping of emitter and the light doping of the base.

Transistor Symbols:-



NPN

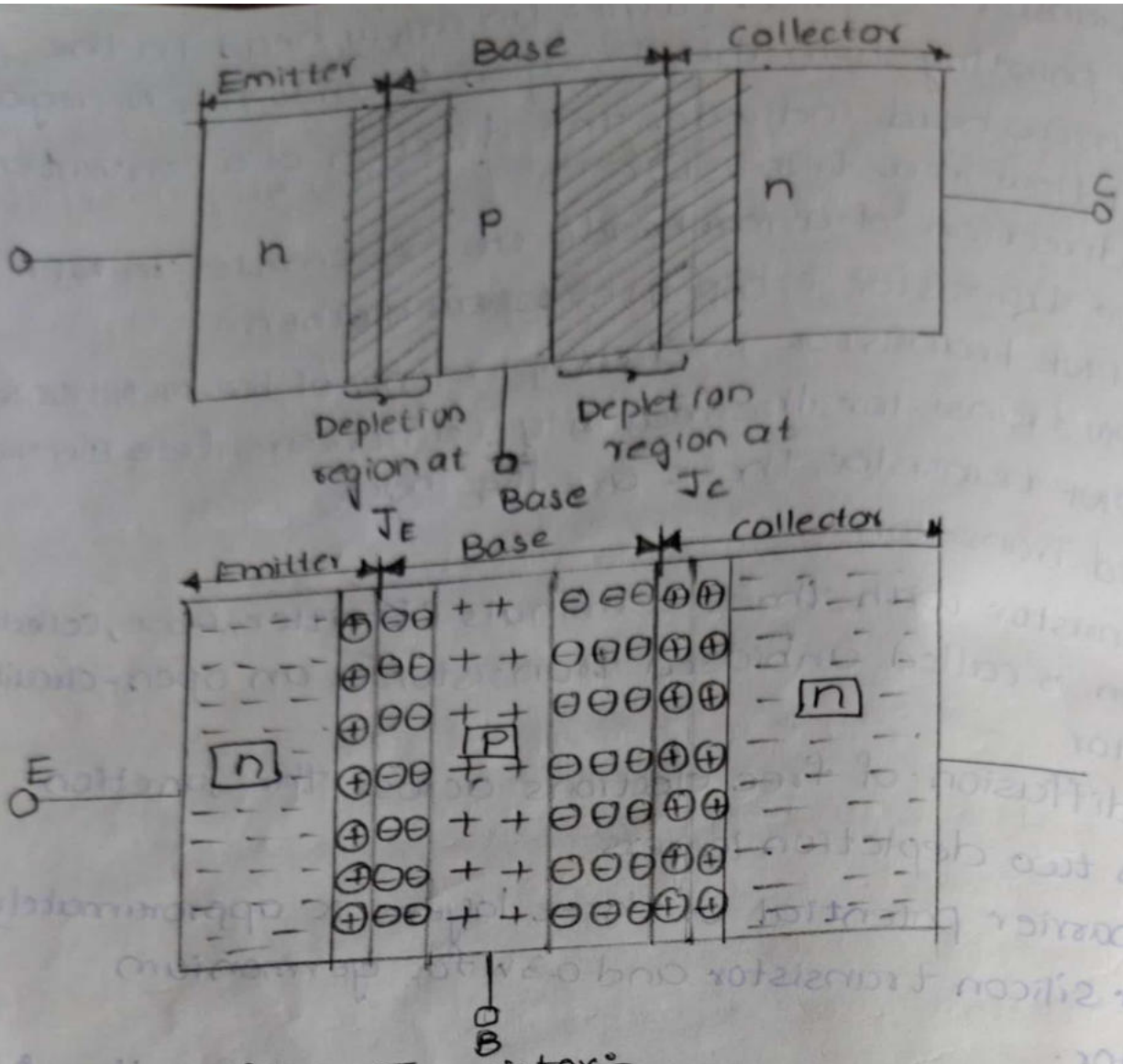


PNP

→ The transistor symbol carries an arrow head in the emitter pointing from the P-region towards the N-region.
→ The arrow head indicates the direction of a conventional current flow in a transistor.
→ The direction of arrow heads at the emitter in NPN and PNP transistor is opposite to each other.
→ The PNP transistor is a complement of the NPN transistor.
→ In NPN transistor the majority carriers are free electrons, while PNP transistor these are the holes.

Unbiased Transistors:-

→ A transistor with three terminals (Emitter, Base, Collector) left open is called unbiased transistor or an open-circuited transistor.
→ The diffusion of free electrons across the junction produces two depletion layers.
→ The barrier potential of three layers is approximately 0.7v for silicon transistor and 0.3v for germanium transistor.
→ Since the regions have different doping levels therefore the layers do not have the same width.
→ The emitter base depletion layer penetrates slightly into the emitter as it is a heavily doped region where as it penetrates deeply into the base as it is a lightly doped region.
→ Similarly the collector-base depletion layer penetrates more into the base region and less into the collector region.
→ The emitter-base depletion layer width is smaller than that of collector base depletion layer.
→ The unbiased transistor is never used in actual practice. Because of this we went for transistor biasing.



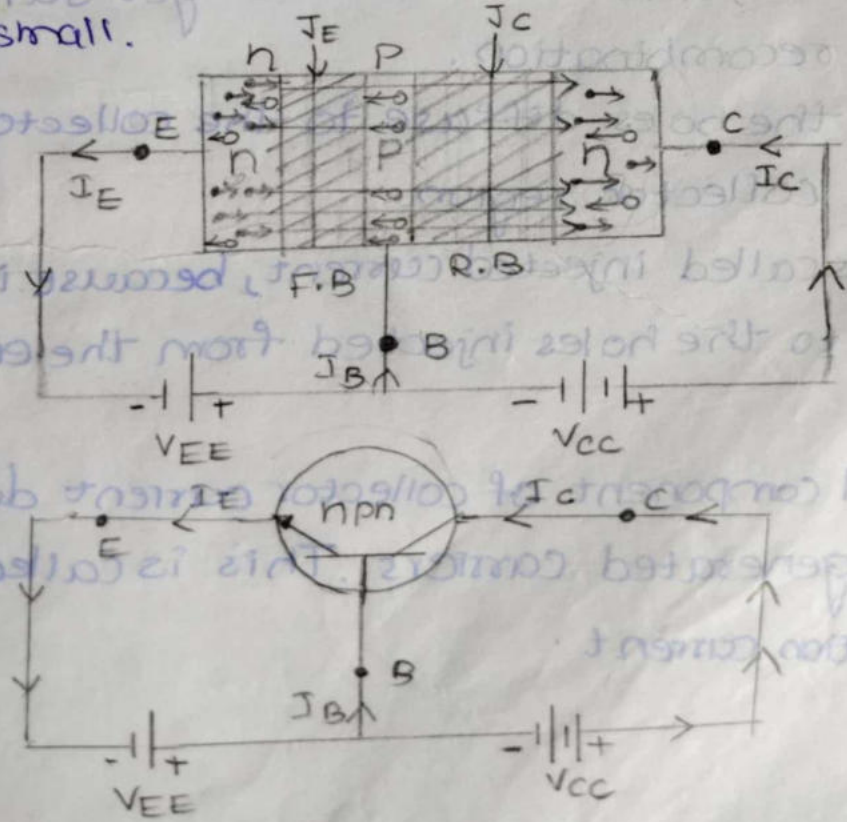
Operation of NPN Transistor:-

→ The NPN transistor is biased in forward active mode i.e, emitter-base of transistor is forward biased and collector base junction is reverse biased.

→ The emitter-base junction is forward biased only if V is greater than barrier potential which is 0.7 V for Silicon and 0.3V for germanium transistor.

→ The forward bias on the emitter-base junction causes the free electrons in the N-type emitter to flow towards the base region. This constitues the emitter current. Direction of conventional current is opposite to the flow of electrons.

> Electrons after reaching the base region tend to combine with the holes.
> If these free electrons combine with holes in the base, they constitue base current.
> Most of the free electrons do not combine with the holes in the base.
> This is because of the fact that the base and the width is made extremely small and electrons do not get sufficient holes for recombination.
> Thus most of the electrons will diffuse to the collector region and constitutes collector current. This collector current is also called injected current, because of this current is produced due to electrons injected from the emitter region.
> There is another component of collector current due to the thermal generated carriers.
> This is called reverse saturation current and is quite small.



Operation of PNP Transistor:-

→ operation of a PNP transistor is similar to npn transistor.

→ The current within the PNP transistor is due to the movement of holes where as in an NPN transistor it is due to the movement of free electrons

→ In PNP transistor, its emitter-base junction is forward biased and collector base junction is reverse biased.

→ The forward bias on the emitter-base junction causes the holes in the emitter region to flow towards the base region. This constitutes the emitter current.

→ The holes after reaching the base region, combine with the electrons in the base and constitue base current.

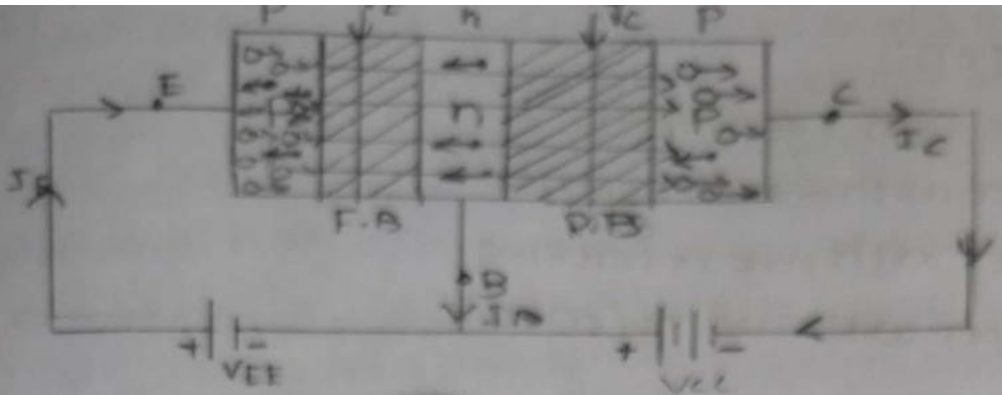
→ Most of the holes do not combine with the electron in the base region.

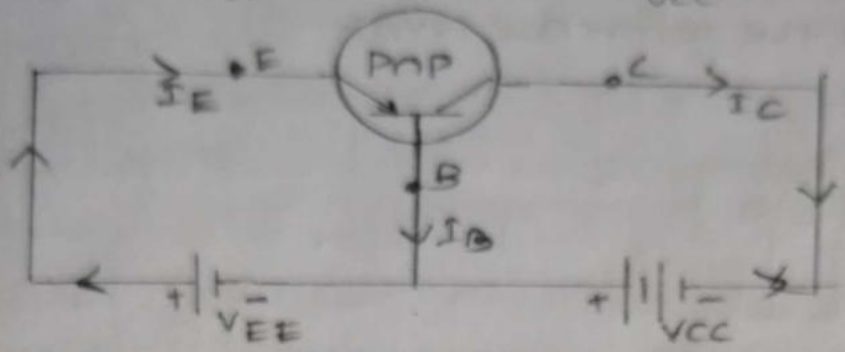
→ This is due to the fact that base width is made extremely small, and holes does not get sufficient electrons for recombination.

→ Thus most of the holes diffuse to the collector regi and constitues collector region.

→ This current is called injected current, because it is produced due to the holes injected from the emitter region.

→ There is small component of collector current due to the thermally generated carriers. This is called reverse Saturation current.





Transistor Currents:-

⇒ We know that direction of conventional current is always opposite to the electron current in any electronic device

⇒ However, the direction of a conventional current is same as that of a hole current in a PNP transistor

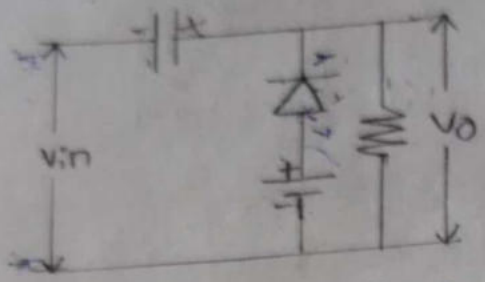
- Emitter current
- Base current
- Collector current

⇒ Since the base current is very small.

Biased clampers:-

1. +ve clamper with +ve reference
2. +ve clamper with -ve reference
3. -ve clamper with +ve reference
4. -ve clamper with -ve refence.

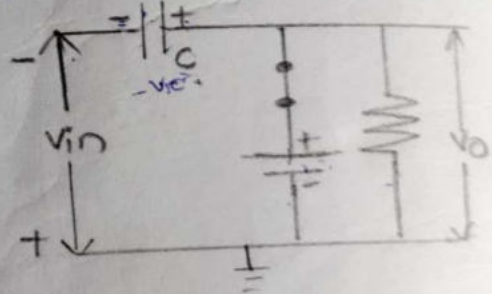
① +ve clamper with +ve reference (+Vr):-



Negative half cycle:- During the negative half cycle of input signal, terminal A becomes negative and terminal B becomes positive. In this case, both input and battery voltages make the diode forward biased.

→ When the diode is in the forward biased condition, the diode will act as closed switch, then the capacitor starts charging and its value is equal to the sum of the input voltage and the bias voltage.

→ This means that the voltage across the capacitor is -Vm+Vr. Moreover in this case, no signal appears at the output, as shown in fig.



Applying KVL

$V_{in} = V_c + V_r$

$V_c = V_{in} - V_r$

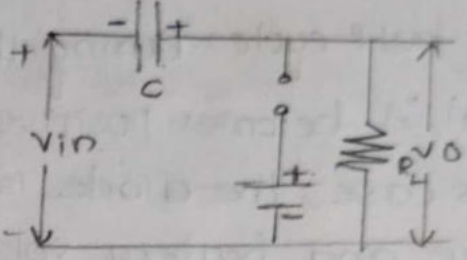
$\boxed{V_c = -V_m - V_r}$

Positive half cycle:- During the positive half cycle of the input signal, terminal 'A' becomes positive and terminal 'B' becomes negative. In this case, the input signal makes the diode reverse biased.

→ At the same time, the battery provides forward bias to the diode.

During +ve half cycle, if $V_m < V_r$, then the diode will act as closed switch because of the forward biased condition of the diode. In this condition, the diode will not allow the input signal to appear across the output. Because of the closed switch action and forward bias condition, the capacitor starts charging.

When $V_{in} > V_r$ the the diode becomes reverse biased, and it will act as an open switch. For this case, the input signal will appear across the output along with the charge present on the capacitor. So, we will get an additional DC shift in the input signal.



Apply KVL:

$V_{in} = V_c + V_o$

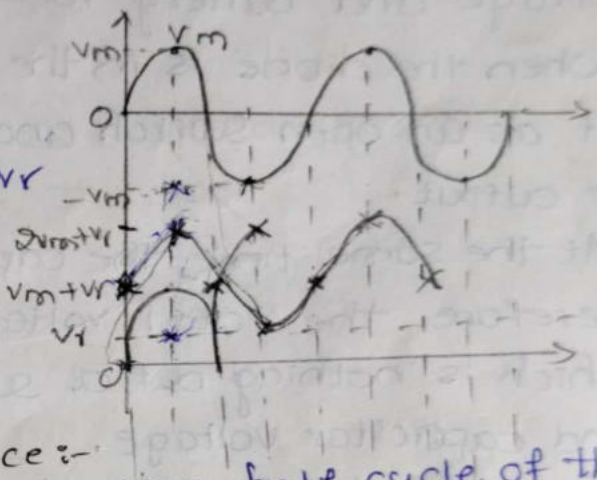
$V_{in} = -V_m - V_r + V_o$

$\boxed{V_o = V_{in} + V_m + V_r}$

case1: If $V_{in} = 0$, $V_o = V_m + V_r$

case2: If $V_{in} = V_m$ then $V_o = 2V_m + V_r$

case3: If $V_{in} = -V_m$ then $V_o = V_r$

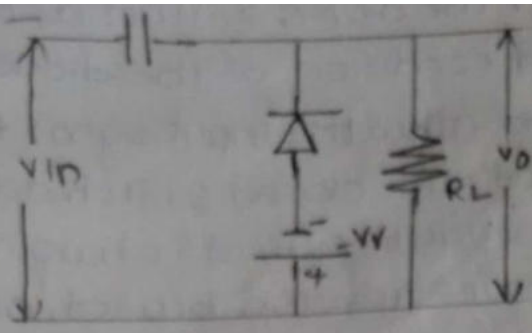


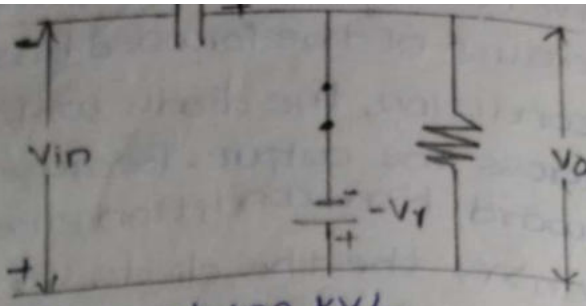
(2) +ve clamper with -ve reference:-

Negative half cycle: During the negative half cycle of the input signal, terminal A becomes negative and terminal B becomes positive. In this case, the diode is forward biased by the input signal and reverse biased by the battery voltage.

→ When the diode is in forward biased condition, the diode will act as a closed switch, then the capacitor starts charging, and its value is equal to difference b/w the peak input voltage and the bias voltage. This means that the voltage across the capacitor is '$-V_m + V_r$'.

→ Moreover, in this case, no signal appears at the output as shown in fig





By applying KVL

During -ve half cycle $V_{in} = V_C + V_\gamma$

$V_C = V_{in} + V_\gamma$

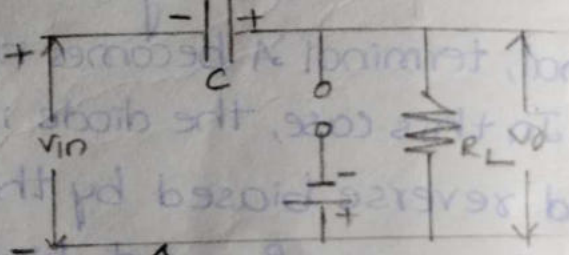
$V_C = -V_m + V_\gamma$

positive half cycle: During the +ve half cycle of the input signal terminal "A" becomes positive and terminal "B" becomes negative. For this case, the diode is reverse biased by both the input voltage and battery voltage.

→ When the diode is in the reverse biased condition, it will act as an open switch and allow the input to appear across the output.

→ At the same time, the capacitor starts discharging, therefore the total voltage appears across the output, which is nothing but a summation of the input voltage and capacitor voltage.

→ Thus, the total voltage V_o becomes the sum of the input and capacitive voltages.



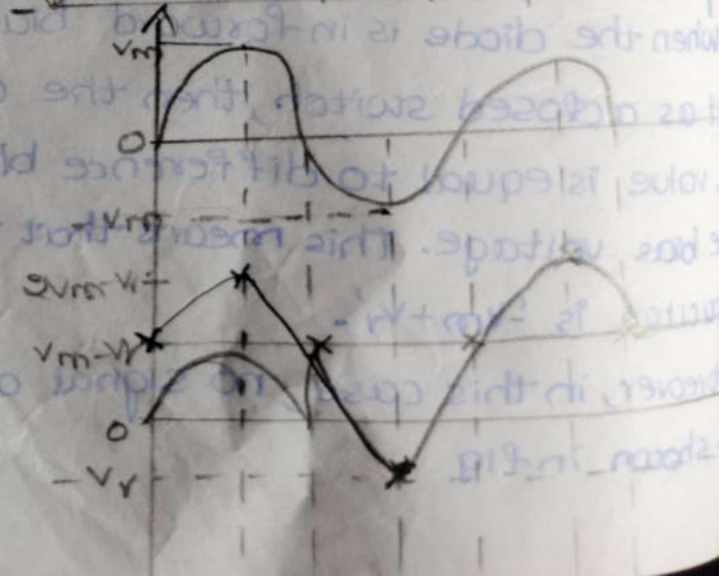
By applying KVL

During +ve half cycle

$V_{in} = V_C + V_o$

$V_{in} = -V_m + V_\gamma + V_o$

$\boxed{V_o = V_{in} + V_m - V_\gamma}$



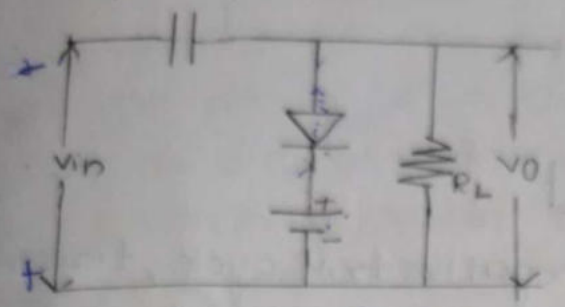
Case (i):

$V_{in} = 0, \quad V_o = V_m - V_\gamma$

$V_{in} = V_m, \quad V_o = 2V_m - V_\gamma$

$V_{in} = -V_m$, $V_o = -V_r$

③ ve clamper with reference (+Vr):



positive halfcycle:- During positive halfcycle of the input signal, terminal "A" becomes positive and terminal "B" becomes negative. For this case, the input signal makes the diode as forward biased. At the same time, the battery provides reverse bias to the diode.

→ Because of the reverse biased condition of the diode, if $V_{in} < V_r$ during the +ve half cycle, the diode will act as an open switch.

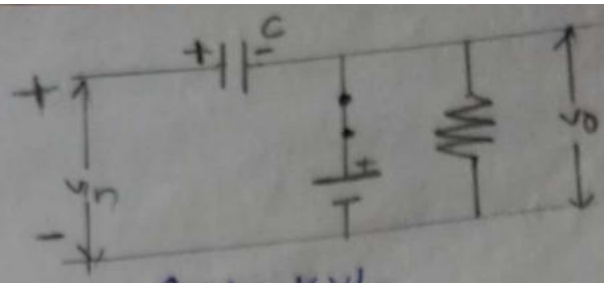
→ For this condition, the diode will not allow the input signal to appear across the output because the diode is connected in parallel.

→ Because of the open switch action and reverse bias condition, the capacitor will not charge.

→ When $V_{in} > V_r$, the diode becomes forward biased, acting as a closed switch and preventing the input signal from appearing across the output.

→ During this condition, the capacitor starts charging and charges up to the peak value of the input signal. For this case, the voltage across the capacitor will be equivalent to difference b/w V_m and V_r.

→ This means that the voltage across the capacitor is equivalent to "$V_m - V_r$".



Apply KVL

$v_{in} = v_c + v_r$

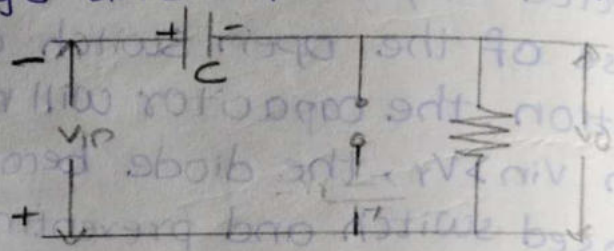
$v_c = v_{in} - v_r$

$\boxed{v_c = v_m - v_r}$

Negative half cycle: During the negative half cycle, terminal A becomes negative and terminal B becomes positive. For this case, the diode will be reverse biased by both the input signal and bias voltage.

→ When the diode is in the reverse biased condition, it will act as an open switch, and the capacitor will start discharging.

→ As a result, whatever the voltage is across the capacitor, it will appear across the output. Moreover, the total voltage across the output is equivalent to the summation of input voltage and capacitor voltage.

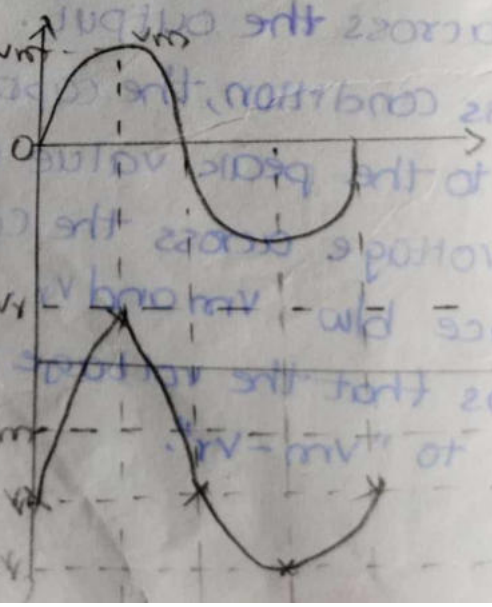


Apply KVL:

$v_{in} = v_c + v_o$

$v_{in} = v_m - v_r + v_o$

$\boxed{v_o = v_{in} - v_m + v_r}$



case i: $v_{in} = 0$ $v_o = -v_m + v_r$

case ii: $v_{in} = v_m$ $v_o = v_r$

case iii: $v_{in} = -v_m$ $v_o = -2v_m + v_r$

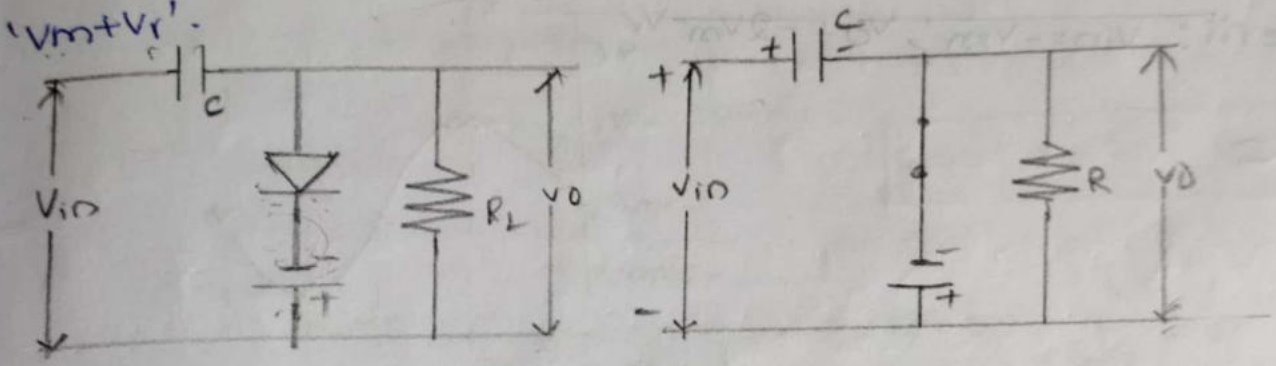
④ -ve clamper with $-V_r$:-

positive half cycle:- During +ve half cycle of the input signal, terminal A becomes positive and terminal B becomes negative.

→ In this case, both the input signal and the bias voltage will forward bias the diode.

→ When the diode is in the forward biased condition, it will act as a closed switch, and the capacitor starts charging with its value equal to the sum of the input voltage and the bias voltage.

→ This means that, the voltage across the capacitor is 'V_m+V_r'.



Applying KVL $V_{in} = V_c - V_r$

$V_c = V_{in} + V_r$

$\boxed{V_c = V_m + V_r}$ [$\because V_{in} = V_m$]

Negative half cycle:- During the negative half cycle of the input signal, terminal "A" becomes -ve and "B" becomes +ve. For this case, the input signal makes the diode as reverse biased.

→ At the same time, the battery provides forward bias to the diode. During -ve half cycle, if $V_{in} < V_r$ the diode will act as closed switch because of the forward biased condition of the diode.

→ For this condition, the diode will not allow the input signal to appear across the output. Because of the closed switch action and forward bias condition, the capacitor starts charging.

→ When $V_{in} > V_r$, then the diode becomes reverse biased, and it will act as an open switch. For this case, the input signal will appear across the output along with the charge present

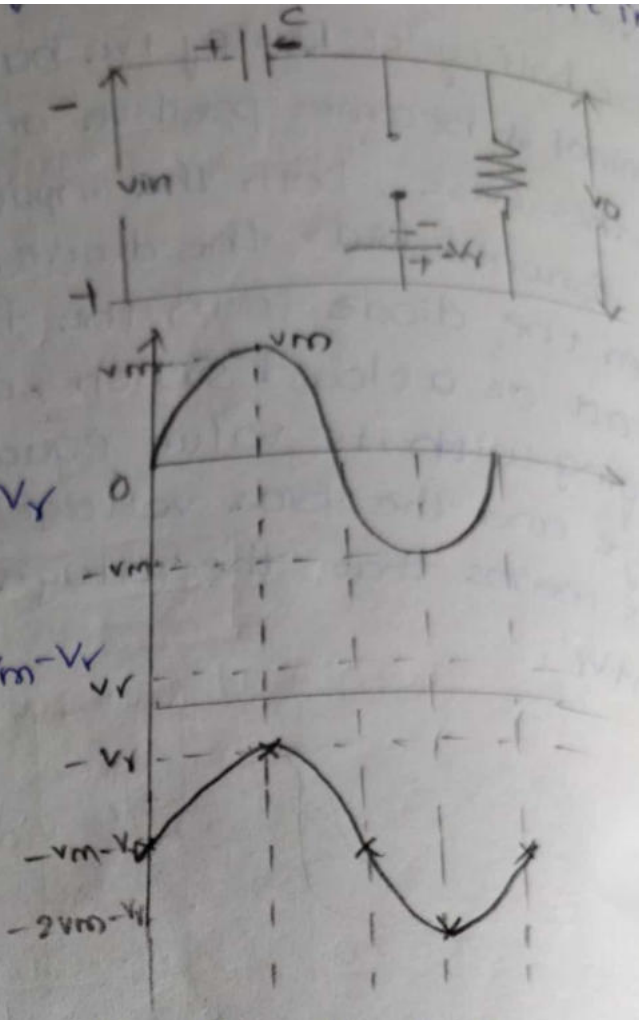
on the capacitor. So,
the input signal.

By applying KVL:-

$V_{in} = V_c + V_o$

$V_{in} = V_m + V_\gamma + V_o$

$\boxed{V_o = V_{in} - V_m - V_\gamma}$



case i: $V_{in} = 0$; $V_o = -V_m - V_\gamma$

case ii: $V_{in} = V_m$; $V_o = -V_\gamma$

case iii: $V_{in} = -V_m$; $V_o = -2V_m - V_\gamma$

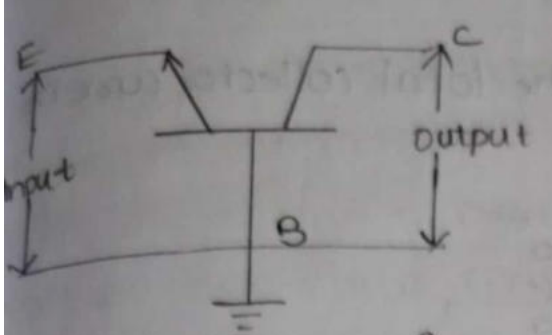
Transistor configurations:

→ Transistor is a three-terminal device, but we require four terminals two for the input and two for the output for connecting it in a circuit.

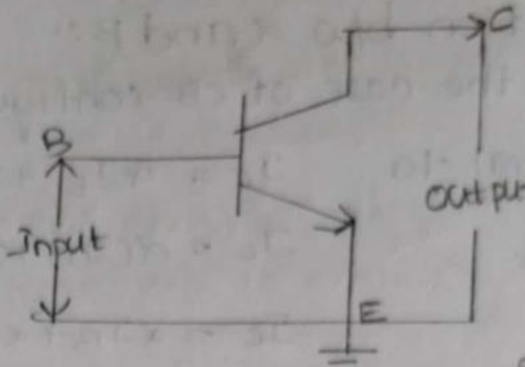
→ Hence, one of the terminals of the transistor is made common to the input and output circuits. Thus there are three types of configurations for operation of a transistor.

→ The three transistor configurations are

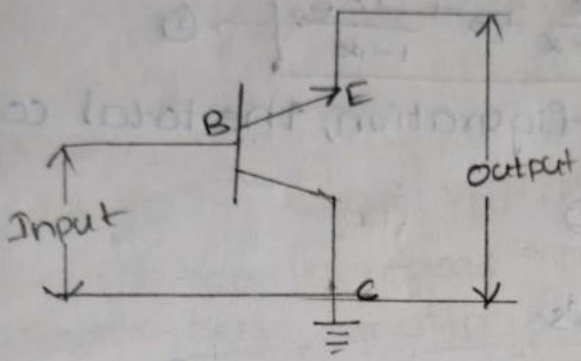
1) common base configuration
2) common emitter configuration
3) common collector configuration



common base configuration

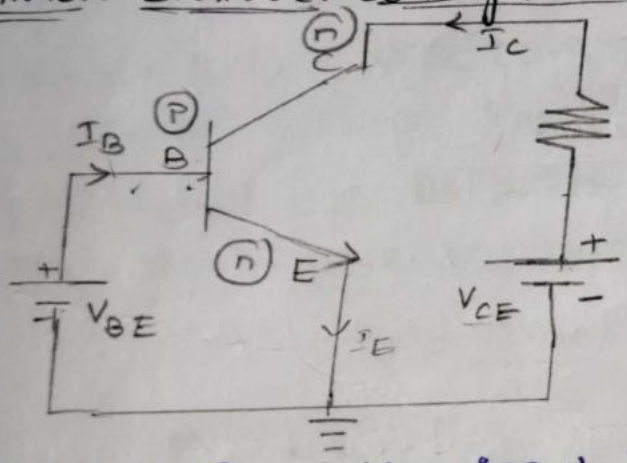


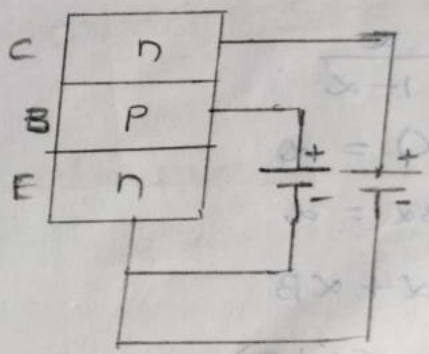
common emitter configuration



common collector configuration

Common Emitter configuration:-





B C E
I_B V_{BE} V_{CC}

⇒ In CE configuration input is connected between base and emitter and output is taken across collector and emitter. In this configuration the base current I_B flows in the input circuit and the collector current I_C flows in the output circuit.

Current amplification factor(β):-

It is defined as the ratio of change in output current to the change in input current.

$$\beta = \frac{\text{change in output current}}{\text{change in input current}}$$

$\beta = \frac{\Delta I_C}{\Delta I_B}$

→ Relation b/w α and β :-

As in the case of CB configuration, the total collector current I_C equal to

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}} \rightarrow (1)$$

As in the case of CE configuration, the total collector cur

$$\boxed{I_C = \beta I_B + I_{CEO}} \rightarrow (2)$$

comparing (1) and (2) eqn's

$$\beta = \frac{\alpha}{1-\alpha}, \quad I_{CEO} = \frac{1}{1-\alpha} I_{CBO} \rightarrow (3)$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta(1-\alpha) = \alpha$$

$$\beta - \beta\alpha = \alpha$$

$$\beta = \alpha + \alpha\beta$$

$$\beta = \alpha(1+\beta)$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}} \rightarrow (4)$$

Substitue (4) in eqn (3)

$$I_{CEO} = \frac{1}{1 - \frac{\beta}{1+\beta}} \cdot I_{CBO}$$

$$= \frac{1+\beta}{1+\beta-\beta} I_{CBO}$$

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}} \rightarrow (5)$$

substitue eqn ④ in ③

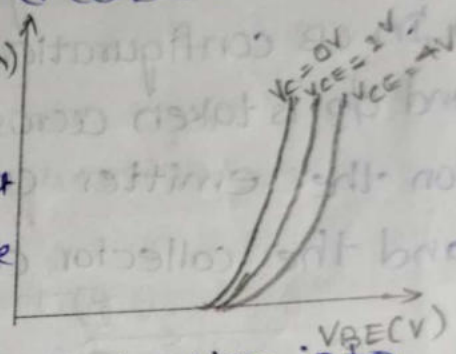
$$I_{CE} = \beta I_B + (1+\beta) I_{CB_0}$$

I/P and o/p characteristics of CE configaration :-

Input characteristics :-

→ The curve drawn between base current I_B and emitter-base voltage V_{BE} for a constant voltage V_{CE} is known as Input characteristics.

→ For a given value of V_{CE} the emitter-base junction is forward biased and acts like P-N junction and conducts current after knee voltage (cut-in voltage)



→ With the increase in V_{CE} causes the i/p current I_B to be lower V_{BE}, because high value of V_{CE} increases reverse bias for collector-base junction and causes greater depletion region and penetration into base which causes the reduction of base space.

→ Inorder to get base current, we have to provide highest base emitter voltage V_{BE}.

→ Input resistance (i) :- The ratio of change in inpult voltage ΔV_{BE} to change in input current ΔI_B.

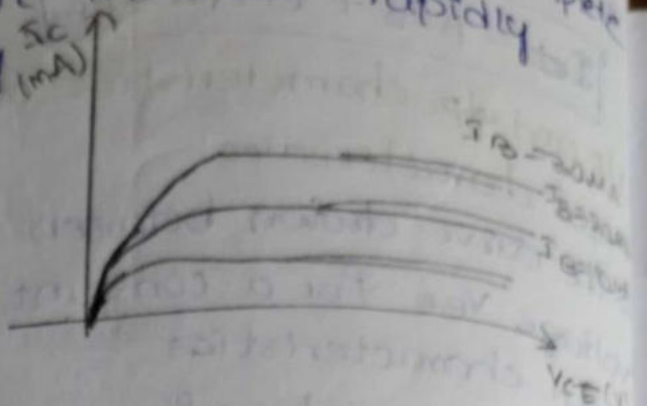
$$R_I = \frac{\Delta V_{BE}}{\Delta I_B}$$

output characteristics :-

→ The curve drawn b/w output voltage V_{CE} and output current I_C at constant input current I_B is known as output characteristics.

→ With the low values of I_B that is 0uA only leak current flows thraugh the collector region. with the low values of V_{CE} base current I_B doesnot cause a corresponding change in collector current I_C.

→ with much values of V_{CE} breakdown and collector current increases rapidly

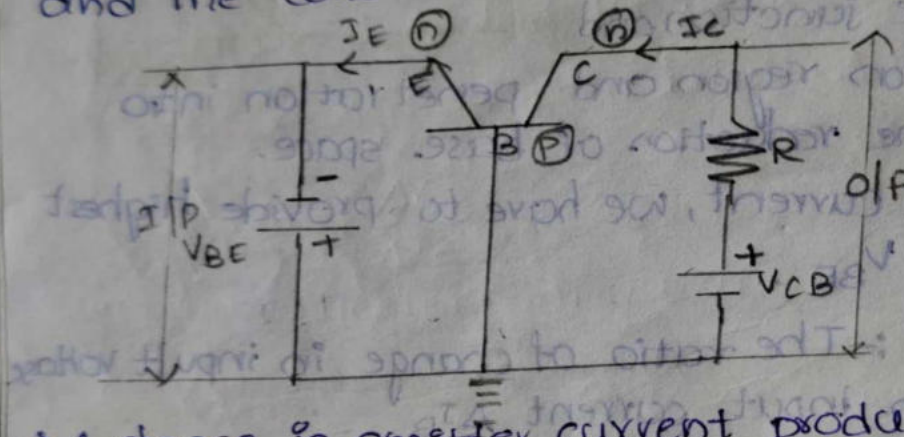


Output resistance (r_o): The ratio of change in o/p voltage ΔV_{CE} to change in o/p current ΔI_C.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Common-base configuration:-

→ In CB configuration i/p is connected b/w emitter and base and o/p is taken across collector and base. In this configuration the emitter current I_E flows in the input circuit and the collector current I_C flows in the o/p circuit.



→ A change in emitter current produces a similar change in collector current.

Current amplification factor (α):-

The ratio of change in o/p current to change in I/p is called current amplification factor (α).

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Expression for collector current (I_C):-

→ The collector current consists of two parts

1) The current produced due to normal transistor act which is produced by majority carriers (αI_E).

ii) The leakage current due to movement of minority across collector-base junction or account of reverse bias.

$$I_C = \alpha I_E + I_{CB_0} \rightarrow (1)$$

We know, $I_E = I_B + I_C \rightarrow (2)$

sub (2) in (1)

$$I_C = \alpha(I_B + I_C) + I_{CB_0}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CB_0}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CB_0}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CB_0}$$

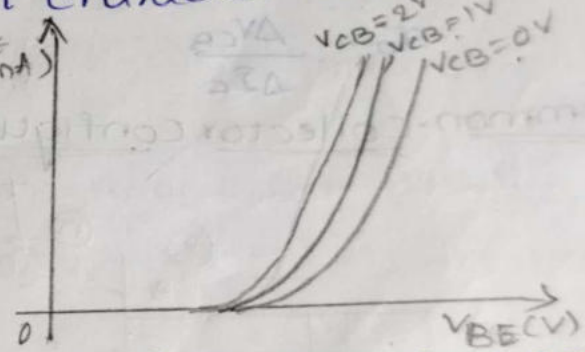
$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} \cdot I_{CB_0}}$$

I/P and O/P characteristics of CB configuration:-

Input characteristics:-

→ The curve drawn between emitter current I_E and emitter base voltage V_{BE} for a given value of collector base voltage V_{BC} is known as input characteristics.

→ For a given value of V_{BC} the emitter-base junction is forward bias and acts like a P-N junction and so the curve is just like P-N junction.



With the increase in V_{CB} the collector base junction experiences a reverse bias and causes the depletion region at collector base junction to penetrate into base of the transistor and reduces the distance b/w emitter-base regions and hence current conduct.

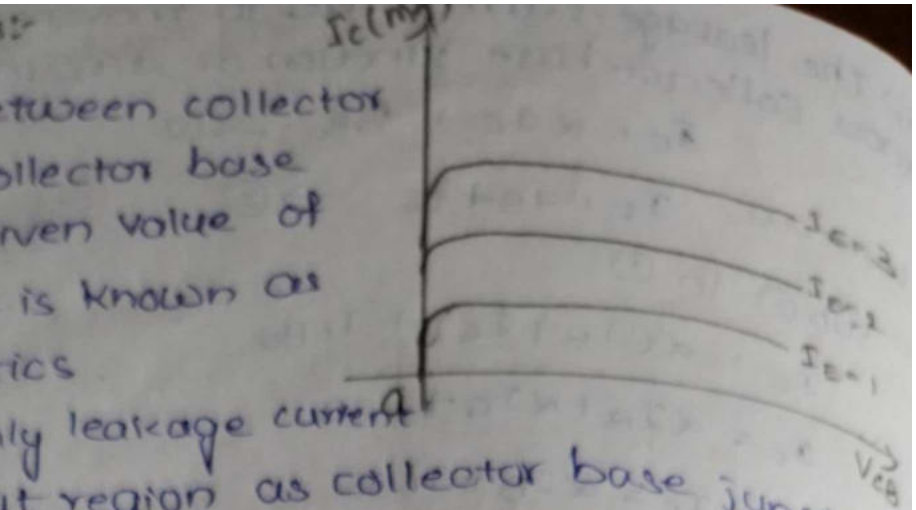
Input resistance (r_i):-

The ratio of change in input voltage ΔV_{BE} to change in input current ΔI_E.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}$$

Output characteristics:-

→ The curve drawn between collector current (I_C) and collector base voltage V_{BC} for a given value of emitter current I_E is known as output characteristics



→ When I_E = 0mA only leakage current flows in the output region as collector base junction is reverse biased.

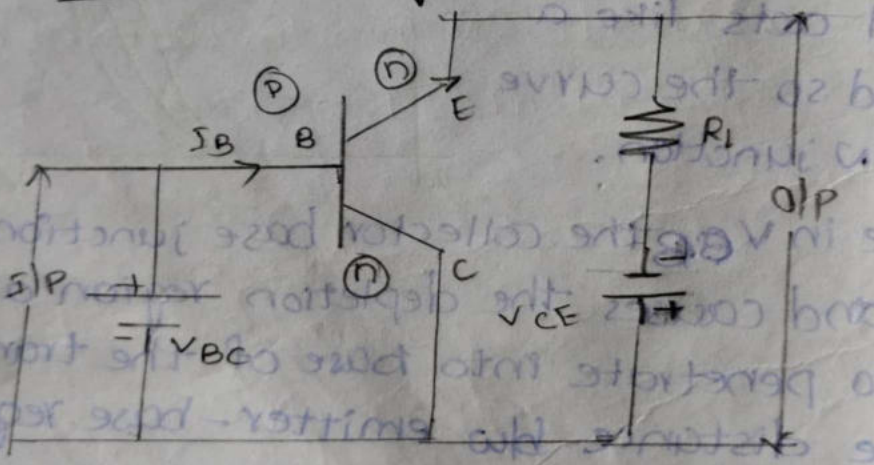
→ With the increase in I_E the collector current I_C is almost equal to I_E and appears to remain constant when V_{CB} is increased.

Output resistance:-

It is defined as the the ratio of change in o/p voltage ΔV_{CB} to change in o/p current ΔI_C

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}$$

Common-Collector configuration:-



→ In cc configuration input is connected between ba and collector output is taken across emitter an collector.

→ In this configuration base current I_B flows in the input circuit and emitter current I_E flows in the output circuit.

current amplification factor (γ):-

It is defined as the ratio of change in output current to change in input current.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relation between α, β and γ:-

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{---(1)}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{---(2)}$$

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \quad \text{---(3)}$$

We know that $I_E = I_B + I_C$ ---(4)

Sub (4) in (3)

$$\gamma = \frac{\Delta(I_B + I_C)}{\Delta I_B}$$

$$\gamma = 1 + \frac{\Delta I_C}{\Delta I_B}$$

$$\boxed{\gamma = 1 + \beta}$$

$$\boxed{\beta = \gamma - 1}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\gamma = 1 + \frac{\alpha}{1-\alpha}$$

$$\gamma = \frac{1-\alpha+\alpha}{1-\alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

$$\gamma(1-\alpha) = 1$$

$$\gamma - \gamma\alpha = 1$$

$$\gamma - 1 = \gamma\alpha$$

$$\boxed{\alpha = \frac{\gamma - 1}{\gamma}}$$

Expression for output current (I_E):

$I_E = I_B + I_C \rightarrow (1)$

From CB configuration,

$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$

Sub (2) in (1)

$I_E = I_B + \alpha I_E + I_{CBO}$

$I_E - \alpha I_E = I_B + I_{CBO}$

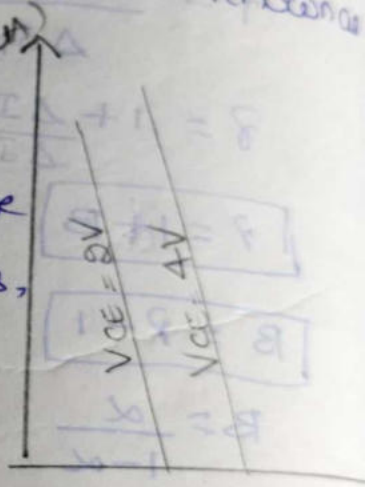
$I_E(1-\alpha) = I_B + I_{CBO}$

$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

Input characteristics:-

→ The curve drawn between collector base voltage and base current by keeping V_{CE} as constant is known as input characteristics



→ With the low value of V_{BC} the base current is more and with the increase in V_{BC} the base current I_B is decreases, because increased V_{BC} will reduce the space of base region

Input resistance (r_i):-

The ratio of change in input voltage ΔV_{BC} to change in input current ΔI_B is known as input resistance

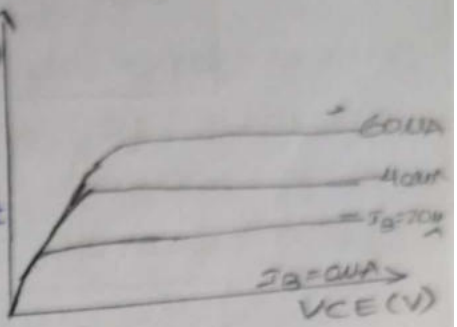
$$\boxed{r_i = \frac{\Delta V_{BC}}{\Delta I_B}}$$

Output characteristics of CC configuration:

→ The curve drawn between collector emitter voltage V_{CE} and emitter current I_E at a constant base current I_B is known as output characteristics.

→ At $I_B = 0\mu A$ only small current flows in the output region which is known as reverse leakage current.

→ From the expression of emitter current ($I_E = \gamma I_B + (1+\gamma) I_{CBO}$) we can say that increased base current will increase the emitter current by 'γ' times of I_B.



Output resistance (r_o):-

It is defined as the ratio of change in output voltage V_{CE} to change in output current I_E is known as output resistance.

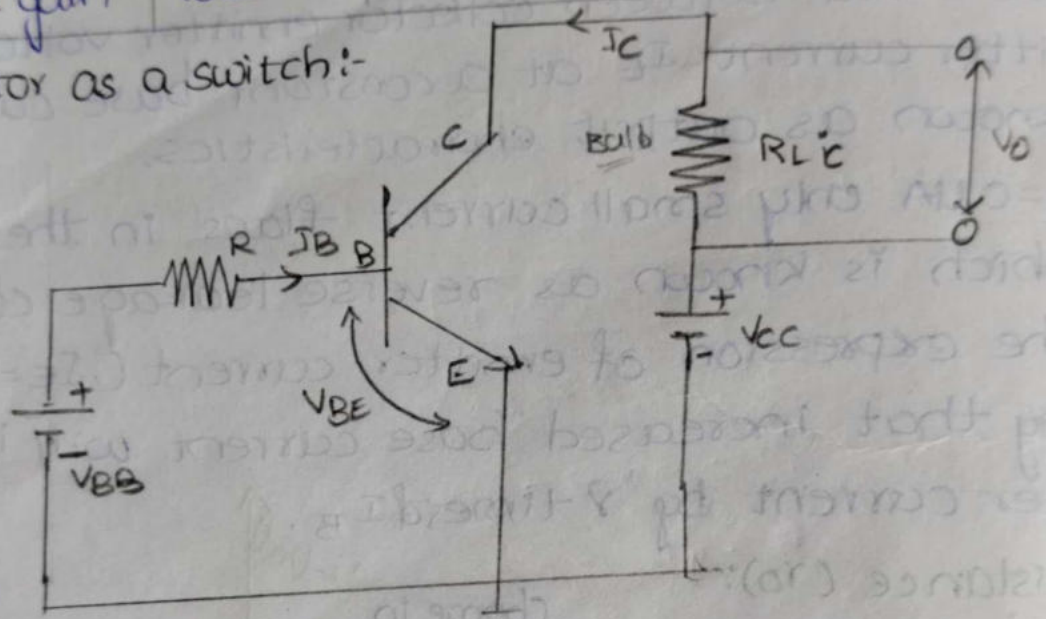
$$r_o = \frac{\Delta V_{CE}}{\Delta I_E}$$

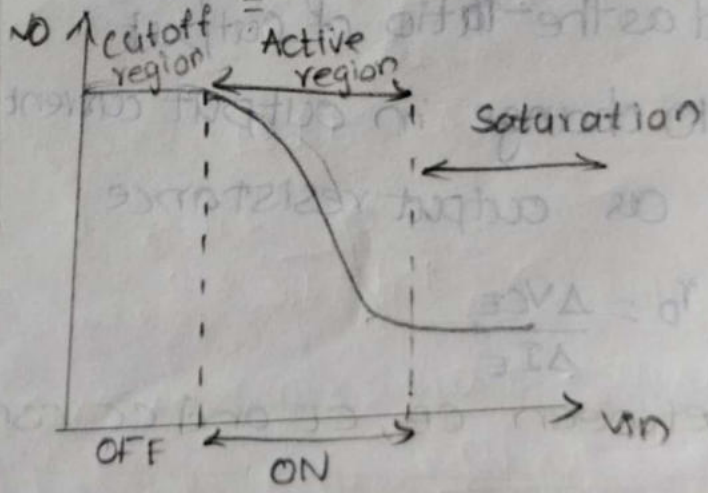
Comparison between CB, CE and CC configurations :-

Parameter	CB configuration (E B C)	CE configuration (B E C)	CC configuration (B C E)
common terminal	Base	Emitter	collector
Input terminal	Emitter	Base	Base
output terminal	collector	collector	Emitter
Input resistance	$r_i = \frac{\Delta V_{BE}}{\Delta I_E}$ low	$r_i = \frac{\Delta V_{BE}}{\Delta I_B}$ medium	$r_i = \frac{\Delta V_{BC}}{\Delta I_B}$ very high
output resistance	$r_o = \frac{\Delta V_{CB}}{\Delta I_C}$ Very high	$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$ high	$r_o = \frac{\Delta V_{CE}}{\Delta I_E}$ low
Current gain	$\alpha = \frac{\Delta I_C}{\Delta I_E}$ less than unity	$B = \frac{\Delta I_C}{\Delta I_B}$ high	$\gamma = \frac{\Delta I_E}{\Delta I_B}$ Very high
Application	High frequency	audio signal amplifier	For impedance matching

voltage gain	low	high	very low

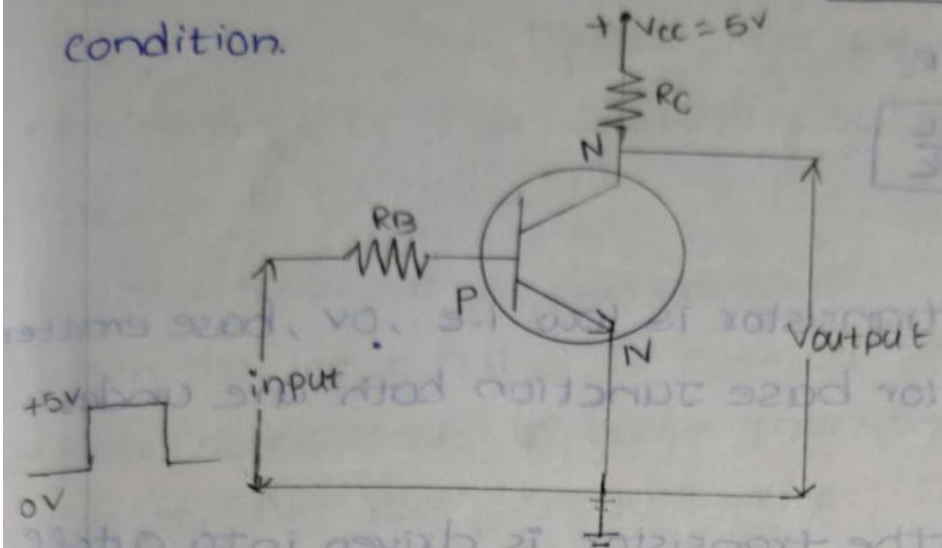
Transistor as a switch:-





Transistor as a switch :-

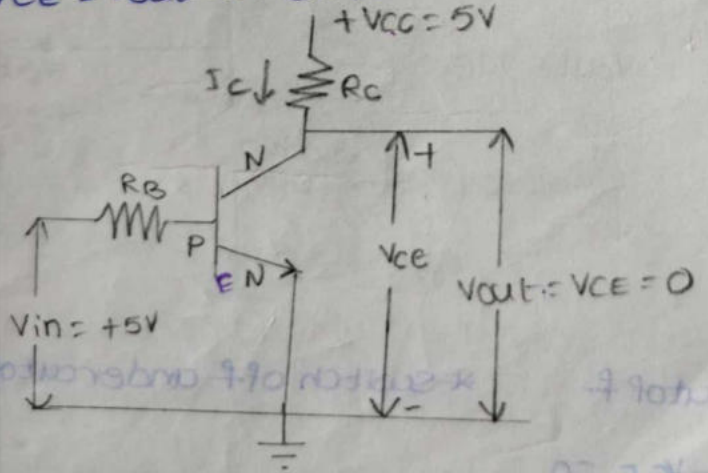
→ In switching circuits, a transistor is operated at cutoff for off condition and at saturation for the ON condition.

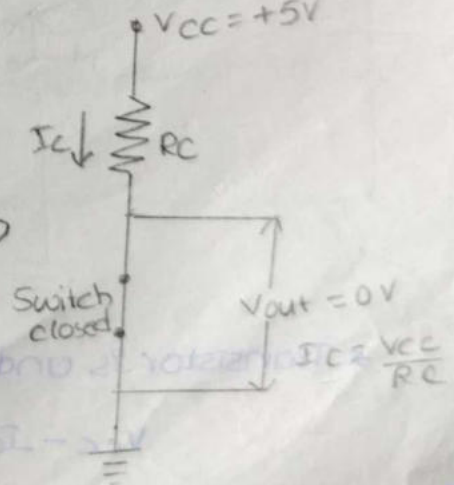


Transistor as a switch

i) **Saturation Region:-** When the input to transistor is high i.e., +5V; the base emitter Junction is forward biased as the transistor is NPN.

At this condition the transistor is driven into saturation and said to be ON & acts as a closed switch. Now, the voltage between collector and emitter is zero (VCE = Vout = 0) and the current is maximum.





* Transistor is saturated

* Switch ON under saturation

→ Apply KVL to the output loop

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CC} = I_C R_C + V_{CE}$ [$\because V_o = V_{CE} = 0$]

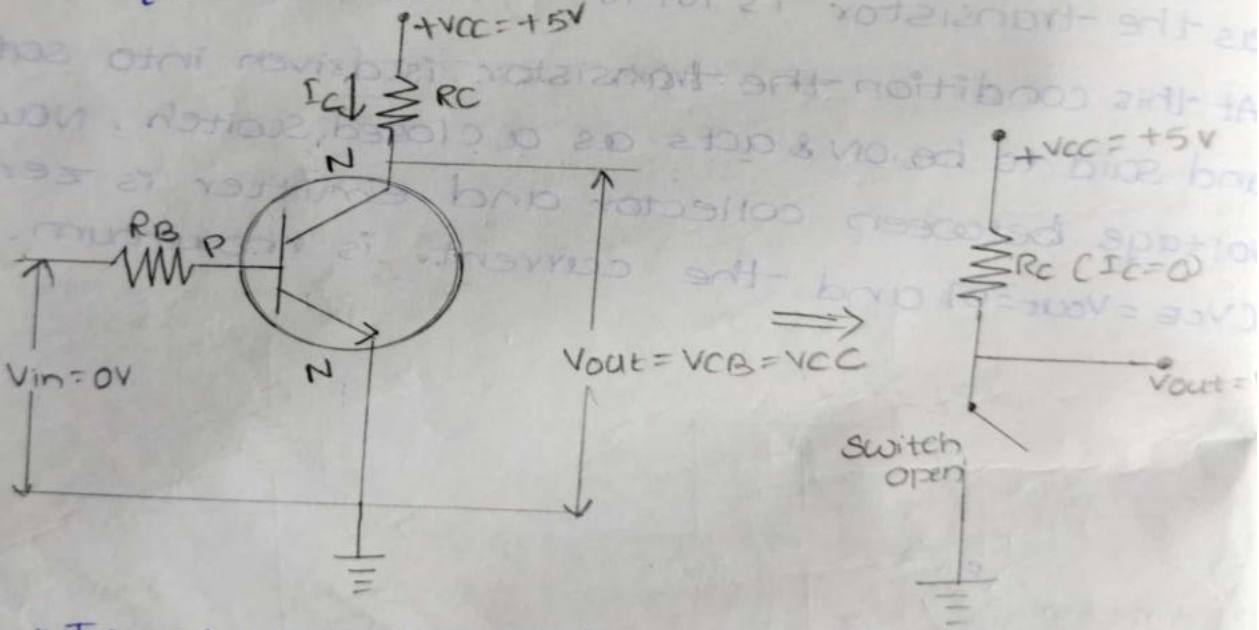
$V_{CC} = I_C R_C$

$$I_C = \frac{V_{CC}}{R_C}$$

ii) Cutoff Region:-

→ When the input to transistor is low i.e., 0V, base em Junction and collector base junction both are unde reverse biased.

→ At this condition, the transistor is driven into cuto and said to be off & acts as a open switch. Now a small current i.e., Negligible current flows through the transistor [$I_C = 0$] and the output voltage Vout will be equal to $+V_{CC}$.



* Transistor is under cutoff

$V_{CC} - I_C R_C - V_{CE} = 0$

$V_{CC} = V_{CE} + I_C R_C$ [$\because I_C = 0$]

$V_{CE} = V_{CC}$

$V_{CE} = +5V$

* Switch off under cutoff

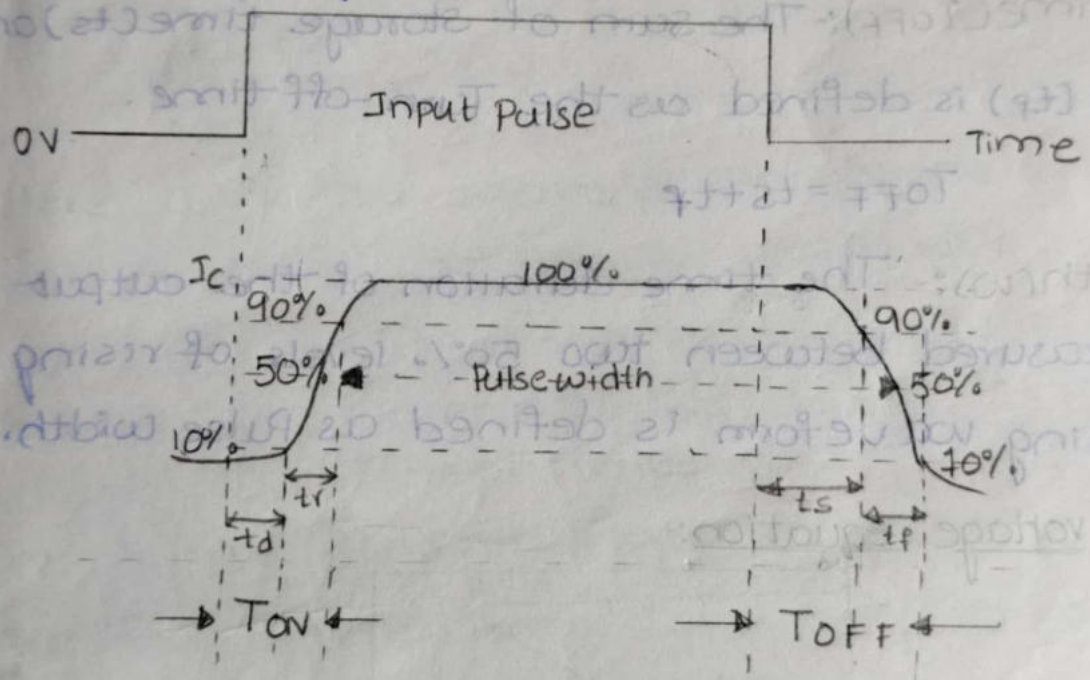
Switching Times:-

The switching transistor has a pulse as an input and a pulse with few variations will be the output. There are a few terms that you should know regarding the timings of the switching output pulse. Let us go through it as below

Let the input pulse duration = T

when the input pulse is applied the collector current takes some time to reach the steady state value, due to the stray capacitances.

The following figure explains this concept.



Output Pulse

From the figure above,

Time delay (td):- The time taken by the collector current to reach from its initial value to 10% of its final value is called as the Time Delay.

Rise time (tr):- The time taken for the collector current to reach from 10% of its initial value to 90% of its final value is called as Rise Time.

Turn-on time (T_{ON}):- The sum of time delay (t_d) and rise time (t_r) is called as Turn-on time.

$$T_{ON} = t_d + t_r$$

Storage time (t_s):- The time interval between the trailing edge of the input pulse to the 90% of the maximum value of the output, is called as the storage time.

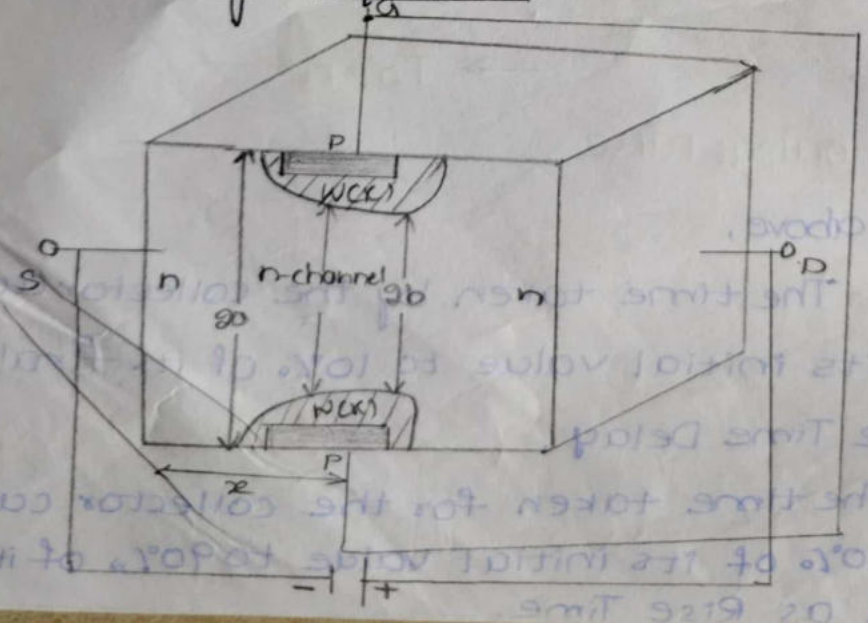
Fall time (t_f):- The time taken for the collector current to reach from 90% of its maximum value to 10% of its initial value is called as the fall Time.

Turn-off time (T_{OFF}):- The sum of storage time (t_s) and fall time (t_f) is defined as the Turn-off time.

$$T_{OFF} = t_s + t_f$$

Pulse width (w):- The time duration of the output pulse measured between two 50% levels of rising and falling waveform is defined as Pulse width.

Pinch off voltage equation:-



$N_A >> N_D$

where N_A is the acceptor ion impurity(holes)

N_D is the Donar ion impurity (electrons)

$W(x) = W_n(x) + W_p(x)$

where $W(x)$ is the p-n junction total depletion region width.

→ Here depletion region pentration is the corrbinatio of n-type channel and p-type gate.

So, $W(x) = W_n(x) + W_p(x)$

$W_p << W_n$

where W_p is very small width compare to W_n so we neglect $W_p(x)$.

$$\boxed{W(x) = W_n(x)}$$

→ $W(x) = a - b(x)$

Here a is the width of the channel and b is width of the channel at drain side.

W is the width of the depletion layer.

b(x) is the parameter defined at the channel width at different value of x.

x is the distance from the source

→ we have already know that junction potential incase of p-n junction diode is

$$V_j = \frac{q N_D W^2}{2\varepsilon}$$

where q is the charge of the electron ($q = 1.6021 \times 10^{-19} C$)

ε = dielectric constant of the channel material

$$W^2 = \frac{2\varepsilon}{q N_D} \cdot V_j$$

$$W = \left[\frac{2\varepsilon}{qN_D} \cdot V_j\right]^{\frac{1}{2}} \longrightarrow (1)$$

But we also know that $V_j = V_o - V_d \longrightarrow (2)$

where V_j is the junction potential

V_o is the contact potential

V_d is the applied voltage (gate channel)

Sub (2) in (1)

$$W = \left[\frac{2\varepsilon}{qN_D}(V_o - V_d)\right]^{\frac{1}{2}}$$

$$W(x) = a - b(x) = \left[\frac{2\varepsilon}{qN_D}(V_o - V_d)\right]^{\frac{1}{2}} \longrightarrow (3)$$

$a - b(x)$ = pentration $W(x)$ of the depletion region in the channel at distance x from the source

Now assume that pinch off has occured then

$b(x) = b = 0$ and $V_d = V_P$

$$W(x) = a - 0 = \left[\frac{2\varepsilon}{qN_D}(V_o - V_P)\right]^{\frac{1}{2}}$$

$$a^2 = \frac{2\varepsilon}{qN_D}(V_o - V_P)$$

$$V_o - V_P = \frac{qN_D}{2\varepsilon} \cdot a^2$$

Here V_o is in microvolts so we can neglect

$$-V_P = \frac{qN_D}{2\varepsilon} \cdot a^2$$

$$|V_P| = \frac{qN_D}{2\varepsilon} a^2 \longrightarrow (4)$$

Relation between V_{GS} and V_P

Put $V_o - V_d = V_{GS}$ in eqn (3)

$$a - b(x) = \left[\frac{2\varepsilon}{qN_D} V_{GS}\right]^{\frac{1}{2}}$$

$$(a-b)^2 = \frac{2\varepsilon}{qN_D} V_{GS}$$

$$V_{GS} = \frac{qN_D}{2\varepsilon}(a-b)^2$$

$$V_{GS} = \frac{qN_D}{2\varepsilon} \cdot \frac{a^2(a-b)^2}{a^2}$$

$$V_{GS} = V_P \cdot \left(\frac{a-b}{a}\right)^2 \quad [\because \text{eq}^n \text{(4)}]$$

$$\boxed{V_{GS} = V_P \left(1 - \frac{b}{a}\right)^2}$$

Problems:-

1. For an n-channel FET with $a = 3\times10^{-4}$ cm, $N_D = 10^{15}$ electron/cubic cm. Find

   i) Pinch off voltage

   ii) The channel half width for $V_{GS} = \frac{1}{2}V_P$ and $I_D = 0$, $\varepsilon_r = 12\varepsilon_0$

Sol:- Given that,

$\varepsilon_r = 12\varepsilon_0$

$a = 3\times10^{-4}$ cm

$N_D = 10^5$ electrons/cubic cm

$V_{GS} = \frac{1}{2}V_P$

where $\varepsilon_0 = 8.854\times10^{-12}$ F/m $\quad q = 1.605\times10^{-19}$

$$V_P = \frac{qN_D \cdot a^2}{2\varepsilon_r}$$

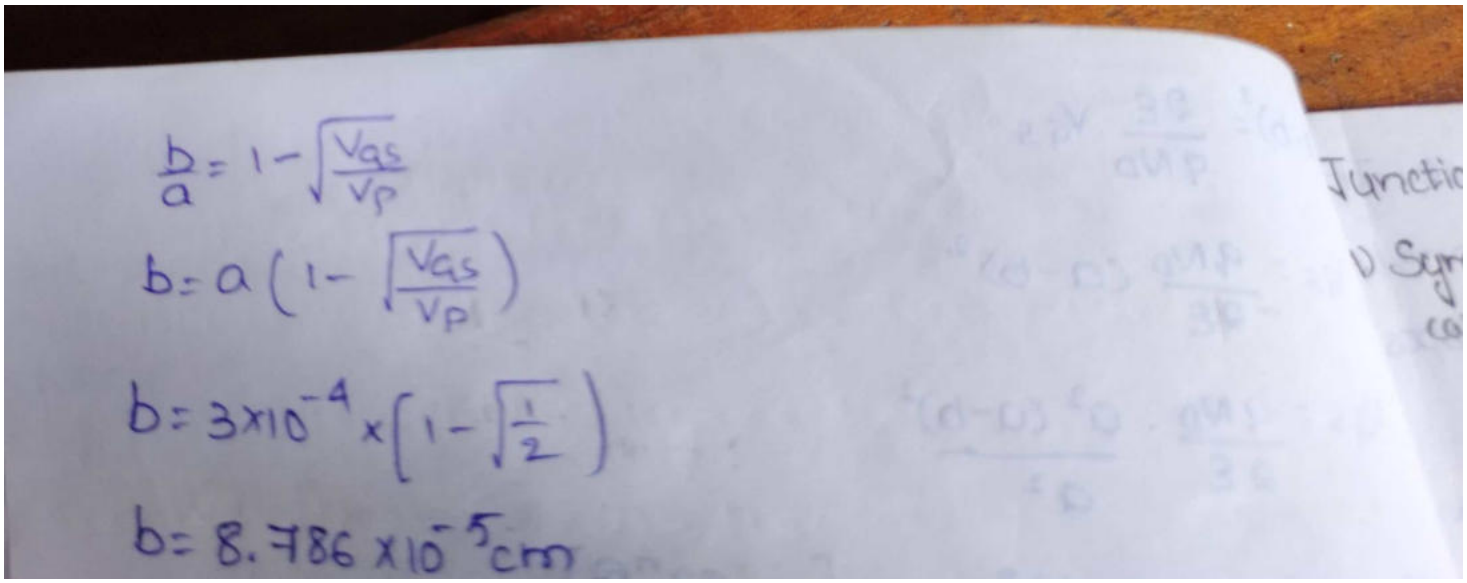
$$= \frac{1.605\times10^{-19}\times10^5}{2\times12\times8.854\times10^{-12}} \times (3\times10^{-4})^2$$

$$= 0.067$$

$$V_{GS} = V_P\left(1-\frac{b}{a}\right)^2$$

$$\frac{V_{GS}}{V_P} = \left(1-\frac{b}{a}\right)^2$$

$$\sqrt{\frac{V_{GS}}{V_P}} = 1 - \frac{b}{a}$$



UNIT-II

Diode Applications

Rectifier: It is an electronic device that converts AC to pulsating DC is known as rectifier. And the process of conversion of Ac to pulsating DC Rectification.

Classification of rectifiers:

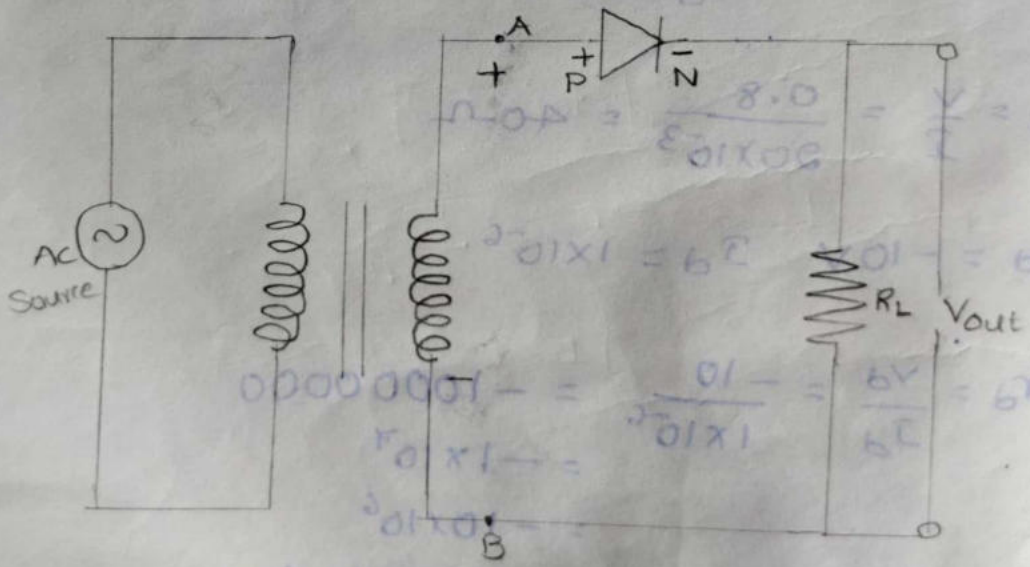
Rectifiers are classified into two categories based on period of conduction.

1. Half wave rectifier
2. Full wave rectifier

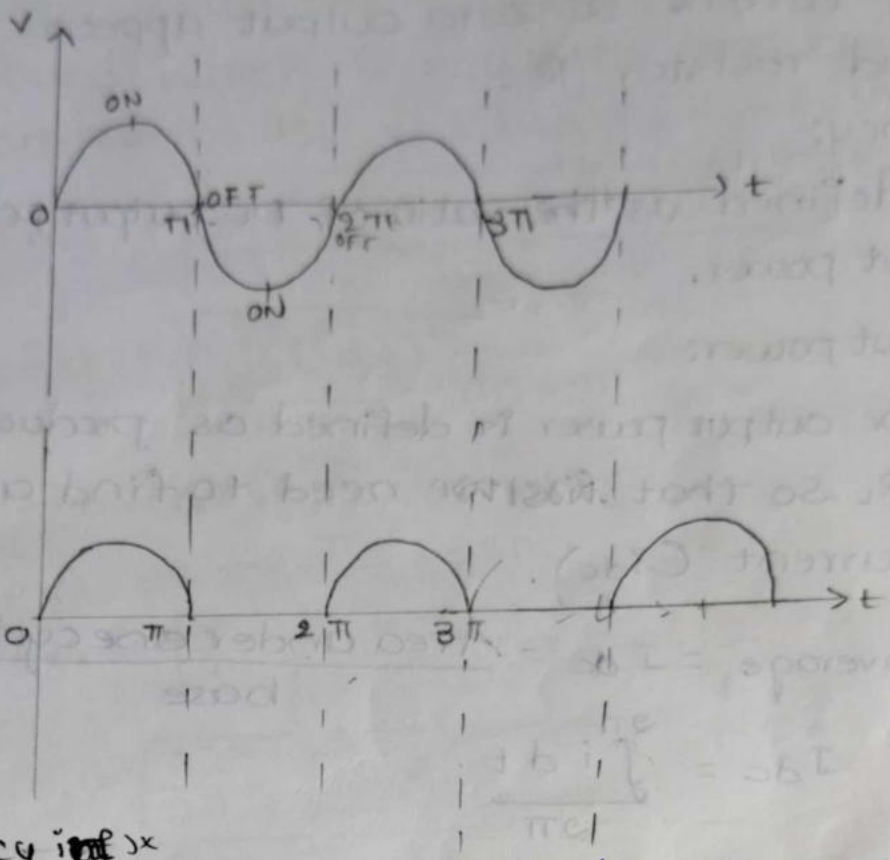
→ Full wave rectifier is further classified into two types. they are

1. centertapped full wave rectifier
2. Bridge full wave rectifier

Half wave rectifier:



Wave forms:



Efficiency of ×

→ A half wave rectifier is one which conducts current during the positive half cycle of the input supply the Ac voltage to be rectified is applied to the input of transformer and the voltage across secondary is available for rectification.

Operation:-

→ During the positive half cycle of the input signal the upperend of secondary winding is positive with respect to lowerend.

→ At this instant diode is forward biased and conducts current so that output appears across the load resistor 'R_L'

→ During the negative halfcycle of the input signal the upperend of the secondary winding is negative with respect to lowerend.

→ At this instant the diode is reverse biased and doesnot conduct current so zero output appears across the load resistor 'R'.

Efficiency:

It is defined as the ratio of DC output power to the AC input power.

DC output power:

The DC output power is defined as product of $i_{dc}^2 \times R_L$. So that we need to find average dc current (i_{dc}).

$$I_{average} = I_{dc} = \frac{\text{Area under one cycle of curve}}{\text{base}}$$

$$I_{dc} = \frac{\int_0^{2\pi} i\,dt}{2\pi}$$

$i = I_m \sin\omega t \; ; \; 0 \le t \le \pi$

$i = 0 \; ; \; \pi \le t \le 2\pi$

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \, d\omega t$$

$$= \frac{I_m}{2\pi}\left[-\cos\omega t\right]_0^{\pi}$$

$$= \frac{-I_m}{2\pi}\left[\cos\pi - \cos 0\right]$$

$$= \frac{-I_m}{2\pi}\left[-1-1\right]$$

$$= \frac{-I_m}{2\pi} \times -2$$

$$= \frac{I_m}{\pi}$$

$$P_{dc} = i_{dc}^2 \times R_L$$

$$P_{dc} = \frac{I_m^2}{\pi^2} \times R_L$$

AC power:-

In order to find the Ac power, ac current has to be found which is equal to rms current.

(Ac input power $P_{AC} = I^2_{rms} \times (R_L + R_f)$).

$$I_{ac} = I_{rms} = \sqrt{\frac{(\text{Area of one cycle of curve})^2}{\text{base}}}$$

$$I_{ac} = \sqrt{\frac{\int_0^{2\pi} (i\,dt)^2}{2\pi}}$$

$i = i_m \sin\omega t \; ; \; 0 \le t \le \pi$

$i = 0 \; ; \; \pi \le t \le 2\pi$

$$I_{rms} = \left[\frac{1}{2\pi} \cdot \int_0^{\pi} i_m^2 \sin^2\omega t \, d\omega t\right]^{\frac{1}{2}}$$

$$= \sqrt{\frac{i_m^2}{2\pi} \int_0^{\pi} \sin^2\omega t \, dt}$$

$$= \sqrt{\frac{i_m^2}{2\pi} \int_0^{\pi} \frac{1-\cos 2\omega t}{2} \cdot dt}$$

$$= \sqrt{\frac{i_m^2}{2\pi}\left[\frac{1}{2}\int_0^{\pi} 1 \cdot dt - \int_0^{\pi} \cos 2\omega t \cdot dt\right]}$$

$$= \sqrt{\frac{i_m^2}{4\pi}\left[[t]_0^{\pi} - \left[\frac{\sin 2\omega t}{2}\right]_0^{\pi}\right]}$$

$$= \sqrt{\frac{i_m^2}{4\pi}[\pi - 0 - 0 + 0]}$$

$$= \sqrt{\frac{i_m^2}{4\pi} \times \pi}$$

$$= \frac{i_m}{2}$$

$$I_{ac} = I_{rms} = \frac{i_m}{2}$$

$P_{ac} = i_{rms}^2 \times (R_L + R_f)$

$P_{ac} = \frac{i_m^2}{2^2} \times (R_L + R_f)$

Efficiency $(\eta) = \frac{P_{dc}}{P_{ac}}$

$$= \frac{\frac{i_m^2}{\pi^2} \times R_L}{\frac{i_m}{2} \times (R_L + R_f)}$$

$$= \frac{i_m^2}{\pi^2} \times R_L \times \frac{1}{\left(\frac{i_m}{2}\right)^2 \times (R_L + R_f)}$$

$$= \frac{\frac{i_m^2}{\pi^2} \times R_L}{\left(\frac{i_m}{2}\right)^2 \times R_L + R_f}$$

$R_f << R_L$

$$= \frac{\frac{i_m^2}{\pi^2} \times R_L}{\frac{i_m^2}{4} \times R_L}$$

$$= \frac{4}{\pi^2}$$

$$= 0.405$$

$$= 40.5\%$$

Ripple factor (γ):-

It is seen that output of half wave rectifier not pure DC but a pulsating dc. The output contains pulsating components called ripples Ideally there should not be any ripples in the rectifier output. The measure of such ripples present in the output is with the help

a factor called ripple factor denoted by γ. It tells how smooth is the output.

$$\text{Ripple factor}(\gamma) = \frac{\text{Rms value of ac component of output}}{\text{average or dc component of output}}$$

Now, the output current is composed of ac component as well as dc component. Let I_{ac} is equal rms value of ac component present in o/p. I_{dc} is equal to dc component present in o/p.

I_{rms} = rms value of total output current.

$$I_{rms} = \sqrt{I_{ac}^2 + (I_{dc})^2}$$

$$(I_{rms})^2 = (I_{ac})^2 + (I_{dc})^2$$

$$(I_{ac})^2 = (I_{rms})^2 - (I_{dc})^2$$

$$I_{ac} = \sqrt{(I_{rms})^2 - (I_{dc})^2}$$

$$\text{Ripple factor}(\gamma) = \frac{\sqrt{(I_{rms})^2 - (I_{dc})^2}}{I_{dc}}$$

$$= \frac{\sqrt{(I_{rms})^2 - (I_{dc})^2}}{\sqrt{(I_{dc})^2}}$$

$$= \sqrt{\frac{(I_{rms})^2 - (I_{dc})^2}{(I_{dc})^2}}$$

$$= \sqrt{\frac{(I_{rms})^2}{(I_{dc})^2} - 1}$$

$$= \sqrt{\frac{(\frac{I_m}{2})^2}{(\frac{I_m}{\pi})^2} - 1}$$

$$= \sqrt{\frac{\pi^2}{4} - 1}$$

$$= \sqrt{\frac{\pi^2 - 4}{4}}$$

$$= \sqrt{\frac{\pi^2 - (2)^2}{(2)^2}}$$

$$= \sqrt{\frac{\pi^2 + 4}{2^2}}$$

$$= \frac{\sqrt{\pi^2 - 4}}{2}$$

$$= 1.211 \times 100$$

$$= 121.03\%$$

→ This indicates that are ripple contents in the output are 1.211 times the dc component that is 121.1% of dc component.

→ The ripple factor for halfwave is very high which not practically indicates that the halfwave circuit is a pure converter of ac to dc.

Problems:

1. A Sinusoidal voltage of peak amplitude of 20 volts is applied to a halfwave rectifier using P-n junction diode with a load resistance of 1000Ω and forward resistance of the diode is 10Ω.
   i) calculate Peak current (I_m), average I_{dc}, I_{Rms}.
   ii) Dc output power.
   iii) Ac input power
   iv) Rectifier efficiency

Sol Given data, $V_m = 20\,V$

$R_L = 1000\,\Omega$

$R_f = 10\,\Omega$

i) $I_m = \frac{V_m}{R_L + R_f} = \frac{20}{1000+10} = \frac{2}{101} = 0.019\,A$

ii) $I_{dc} = \frac{i_m}{\pi} = \frac{0.019}{3.14} = 6.047 \times 10^{-3}\,A$

$I_{ac} = \frac{i_m}{2} = \frac{0.019}{2} = 9.5 \times 10^{-3}\,A$

iii) $P_{dc} = i_{dc}^2 \times R_L$

$= (6.047 \times 10^{-3})^2 \times 1000$

$= 0.0365\,W$

iii) $P_{ac} = i_{ac}^2 \times (R_L + R_f)$

$= (9.5 \times 10^{-3})^2 \times (1000+10)$

$= 0.0911\,W$

iv) Rectifier efficiency $= \frac{P_{dc}}{P_{ac}} = \frac{0.0365}{0.0911}$

$= 0.400 \times 100$

$= 40.06\,\%$

2. An ac supply of 230 volts is applied to a half wave rectifier circuit through of a transformer of turns ratio 5:1. Find DC output voltage

i) Dc output voltage

ii) Efficiency (Assume that the diode to be ideal).

$V_{rms} = 230$ Volts

$N_1 : N_2 = 5 : 1$

$V_m = \sqrt{2} \times V_{rms}$

$v_m = \sqrt{2} \times 230$

$V_m = 325.26\ V$

Secondary maximum voltage $= \frac{N_2}{N_1} \times V_m$

$= \frac{1}{5} \times 325.26$

$v_m = 65.05\ V$

$I_{dc} = \frac{i_m}{\pi} \rightarrow (1)$

$i_m = \frac{V_m}{R_L + R_f} = \frac{V_m}{R_L} \quad (\because R_f << R_L) \rightarrow (2)$

sub (2) in (1)

$I_{dc} = \frac{V_m}{\pi R_L}$

$V_{dc} = I_{dc} \times R_L$

$= \frac{V_m}{\pi R_L} \times R_L$

$= \frac{V_m}{\pi}$

$V_{dc} = \frac{65.05}{\pi} = 20.71\ V.$

ii) Efficiency $= \frac{P_{dc}}{R_{ac}}$

$= \frac{I_{dc}^2 \times R_L}{I_{ac}^2 \times (R_L + R_f)}$

$= \frac{\left(\frac{V_m}{\pi R_L}\right)^2 \times R_L}{\left(\frac{V_m}{2R_L}\right)^2 \times R_L}$

$\left[\because I_{ac} = \frac{I_m}{2}, \quad I_m = \frac{V_m}{R_L}, \quad I_{ac} = \frac{V_m}{2R_L}\right]$

$= \frac{4}{\pi^2}$

$= 40.5\%$.

3. Determine the secondary voltage of transformer to deliver dc power of 1 Watt for 1000Ω load for a halfwave rectifier.

Given $P_{dc} = 1$ watt

$R_L = 1000\Omega$

$P_{dc} = I_{dc}^2 \times R_L$

$1 = I^2_{dc} \times 1000$

$I_{dc}^2 = \frac{1}{1000}$

$I_{dc}^2 = 1 \times 10^{-3}$

$I_{dc} = \sqrt{1 \times 10^{-3}}$

$I_{dc} = 0.031\,A$

$I_{dc} = \frac{im}{\pi}$

$0.031 = \frac{im}{\pi}$

$im = 0.097\,A$

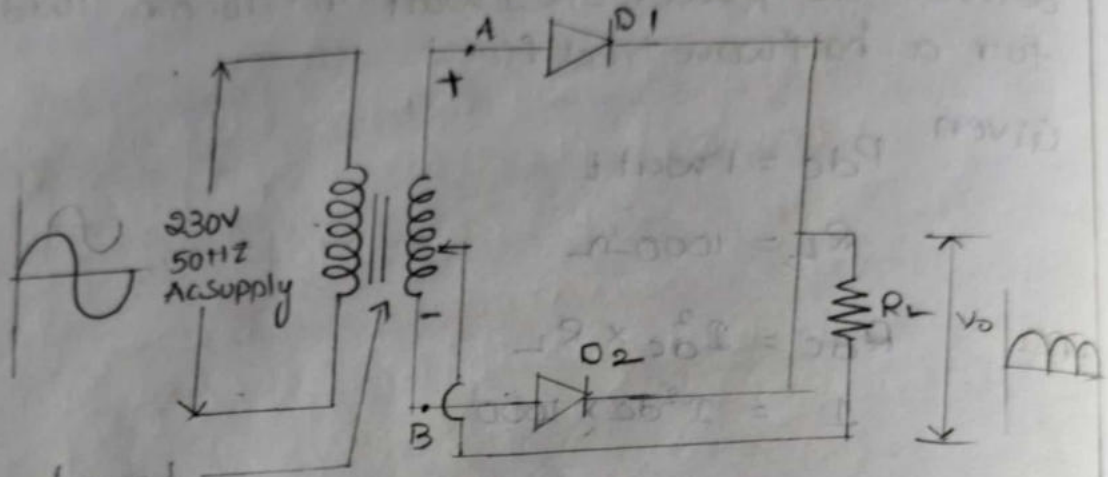
$\left(V_m = \frac{im}{R_L} = \frac{0.097}{1000} = 9.7 \times 10^{-5}\right) \times$

$V_m = im \times R_L = 0.097 \times 1000 = 97\,V$

$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{97}{\sqrt{2}} = 68.58\,V$

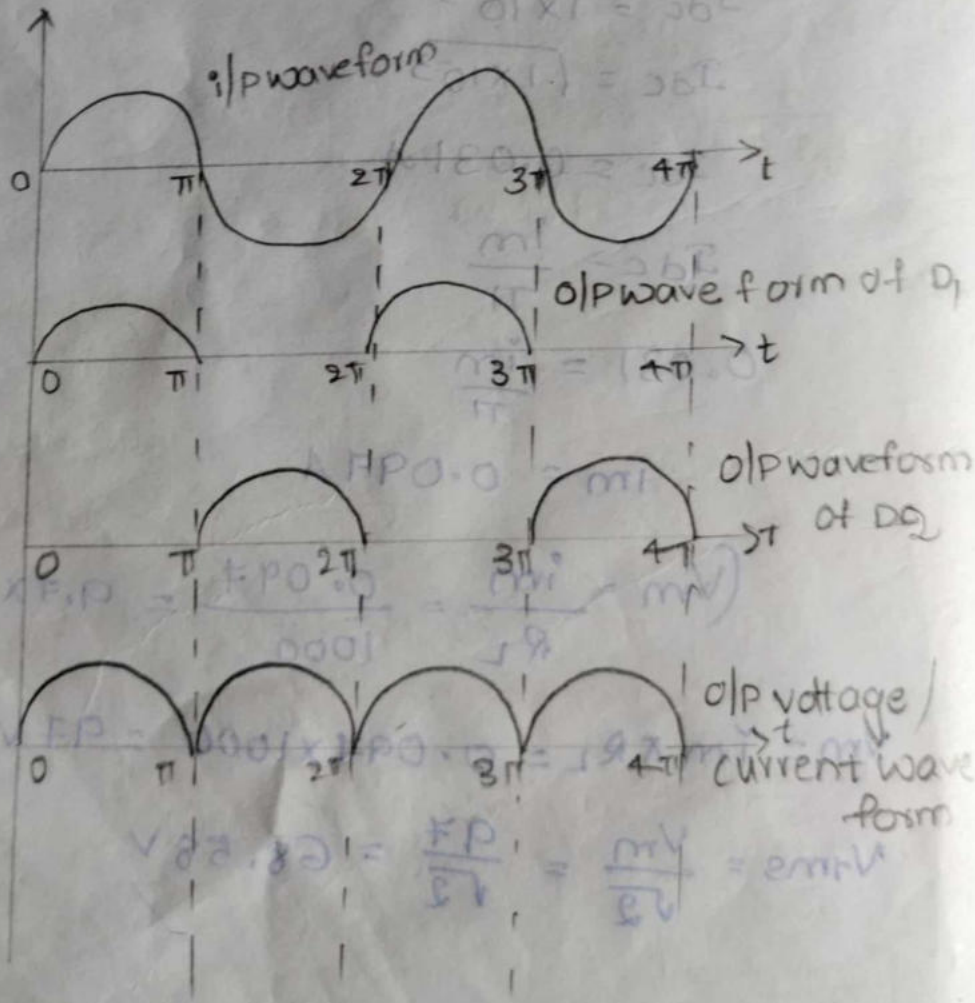
Full wave Rectifier:-

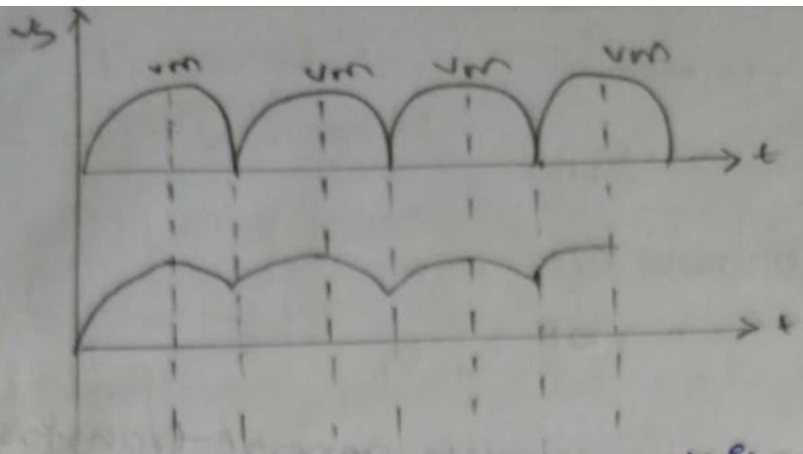
i) center tapped full wave rectifier:-



center tapped transformer

Half wave.





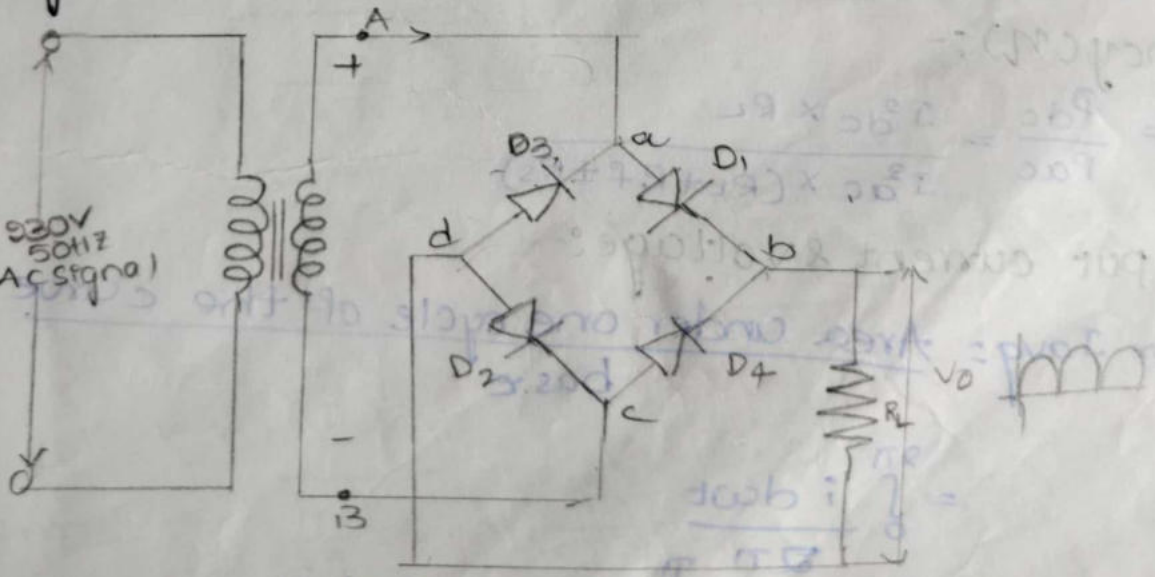
→ Center tapped full wave rectifier consists of center tapped transformer, two diodes named as D_1 and D_2 and load resistor R_L.

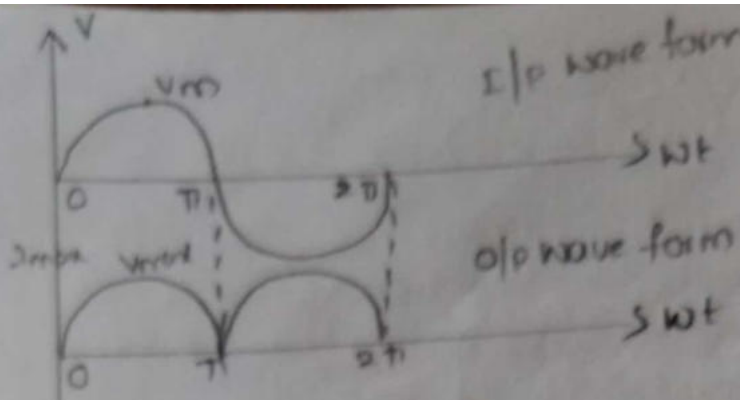
→ During positive half cycle, input signal end A becomes positive with respect to end B at this instant D_1 is in forward bias and D_2 is in reverse bias so current conduction starts by diode D_1 through the path AD_1R_L so the output appears across load resistor R_L.

→ During negative half cycle of the input signal end B becomes positive with respect to end A at this instant D_2 is forward bias and D_1 is reverse bias so current conduction starts by diode D_2 through the path BD_2R_L so the output appears across load resistor R_L.

MIP-1 JNP

ii) Bridge rectifier (full wave) :-





→ Bridge full wave rectifier consists general transformer four diodes named D_1, D_2, D_3 & D_4 and load resistor
→ During positive half cycle of the input of signal upp end of secondary winding becomes positive with respect to lower end at this instant diodes D_1 and conduct as they are in forward bias and output appears across load resistor R_L.
→ During positive half cycle the current flow the path aD1bRLC.
→ During negative half cycle of the input signal lowe end secondary winding becomes positive with resp to upper end at this instant diodes D_3, D_4 conduc as they are in forward bias and output appear across load resistor R_L.
→ During negative half cycle the current flow the path dD4bRLCD3. (C→bRLdD3a)

Efficiency(η):-

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 \times R_L}{I_{ac}^2 \times (R_L + R_f + R_s)}$$

DC output current & voltage:-

I_{dc} or I_{avg}: $\frac{\text{Area under one cycle of the curve}}{\text{base}}$

$$= \int_0^{2\pi} \frac{i\, d\omega t}{2\pi}$$

$$= \frac{1}{2\pi} \times 2 \int_0^{\pi} i_m \sin\omega t\, d\omega t$$

$= \frac{im}{\pi}[-\cos\omega t]_0^{\pi}$

$= -\frac{im}{\pi}[\cos\pi - \cos 0]$

$= -\frac{im}{\pi}[-1-1]$

$= -\frac{im}{\pi} \times -2$

$$\boxed{I_{dc} = \frac{2im}{\pi}}$$

$V_{dc} = V_{avg} = I_{dc} \times R_L$

$= \frac{2im}{\pi} \times R_L$

$= \frac{2V_m}{\pi R_L} \times R_L \quad [\because im = \frac{V_m}{R_L}]$

$$\boxed{V_{avg} = \frac{2V_m}{\pi}}$$

$P_{dc} = I_{dc}^2 \times R_L$

$= \left(\frac{2im}{\pi}\right)^2 \times R_L$

$$\boxed{P_{dc} = \frac{4im^2}{\pi^2} \times R_L}$$

AC input current & Voltage:-

$$I_{rms} \text{ or } I_{ac} = \sqrt{\frac{(\text{Area under one cycle of the curve})^2}{\text{base}}}$$

$= \sqrt{\int_0^{2\pi} \frac{i^2 d\omega t}{2\pi}}$

$= \sqrt{\frac{1}{2\pi} \times 2 \int_0^{\pi} im^2 \sin^2\omega t \cdot d\omega t}$

$= \sqrt{\frac{im^2}{\pi} \int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t}$

$= \sqrt{\frac{im^2}{2\pi} \left[\int_0^{\pi} 1 \cdot d\omega t - \int_0^{\pi} \cos 2\omega t \, d\omega t\right]}$

$= \sqrt{\frac{im^2}{2\pi} \left[[\omega t]_0^{\pi} - \left[\frac{\sin 2\omega t}{2}\right]_0^{\pi}\right]}$

$= \sqrt{\frac{im^2}{2\pi}[[\pi - 0] - 0 + 0]}$

$I_{rms} = \sqrt{\frac{im^2}{2\pi} \times \pi} = \frac{im}{\sqrt{2}}$

$V_{rms} = i_{rms} \times R_L$

$= \frac{i_m}{\sqrt{2}} \times R_L$

$= \frac{v_m}{R_L + R_s + R_f} \times \frac{R_L}{\sqrt{2}}$ $\left[\because i_m = \frac{v_m}{R_L + R_s + R_f}\right]$

$= \frac{v_m}{R_L} \times \frac{R_L}{\sqrt{2}}$ $[\because R_s + R_f << R_L]$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

$P_{ac} = I_{ac}^2 \times (R_L + R_f + R_s)$

$= \left(\frac{i_m}{\sqrt{2}}\right)^2 \times (R_L + R_f + R_s)$

$$\boxed{P_{ac} = \left(\frac{i_m}{\sqrt{2}}\right)^2 \times R_L} \quad (\because R_f + R_s << R_L)$$

$$\text{Efficiency } (\eta) = \frac{P_{dc}}{P_{ac}} = \frac{\frac{4 i_m^2}{\pi^2} \times R_L}{\frac{i_m^2}{2} \times R_L}$$

$$\eta = \frac{8}{\pi^2}$$

$$\eta = 0.8114$$

$$\boxed{\eta\% = 81.1\%}$$

Ripple factor (γ):-

$$\gamma = \frac{I_{ac}}{I_{dc}}$$

$$I_{rms} = \sqrt{I_{ac}^2 + I_{dc}^2}$$

$$I_{ac} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{ac}^2}}{I_{dc}^2}$$

$$= \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$= \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$= \sqrt{\frac{\left(\frac{I_m}{\sqrt{2}}\right)^2}{\left(\frac{2I_m}{\pi}\right)^2} - 1}$$

$$= \sqrt{\frac{\frac{I_m^2}{2}}{\frac{4I_m^2}{\pi^2}} - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$= 0.483$$

$$\boxed{\gamma = 48.3\%}$$

Advantages of half wave rectifier:-

1. Simple construction
2. Less no of components are required.
3. Small size

Disadvantages of half wave rectifier:-

1. More amount of ripple content
2. Rectification efficiency is low.
3. low output voltage or current.
4. Generates harmonics

Advantages of centertopped full wave rectifier:-

1. The dc load voltage and current are more than half wave.
2. The efficiency is higher.
3. The ripple factor is less.
4. The large dc power output.

Disadvantage of center tapped full wave rectifier:-

1. It is difficulty to locate the center tap on Secondary winding.
2. The DC output is small as each diode utilizes only one half of the transformer Secondary voltage.
3. The diode must have high peak inverse voltage.

Advantages of Bridge full wave rectifier:-

1. No center tap is needed in the transformer Secondary winding.
2. The peak inverse voltage is one half that of center tapped circuit.
3. The output is twice that of the Secondary tapped circuit for the same Secondary voltage.

Disadvantages of Bridge full wave rectifier:-

1. It requires four diodes.
2. As during each half cycle of the ac input the two diodes that are conducting series will drop twices× voltage twice.

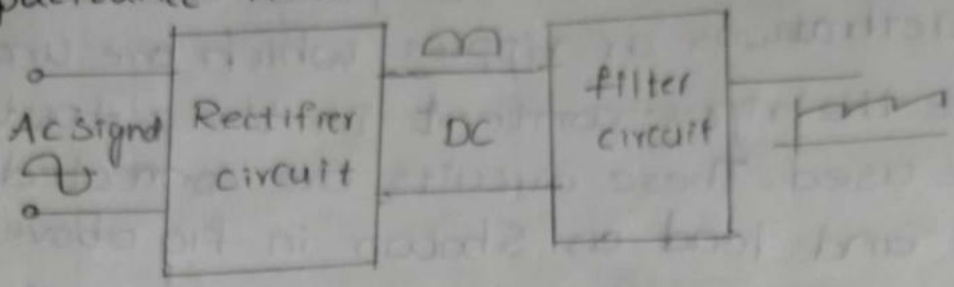
MIO-1
IMD

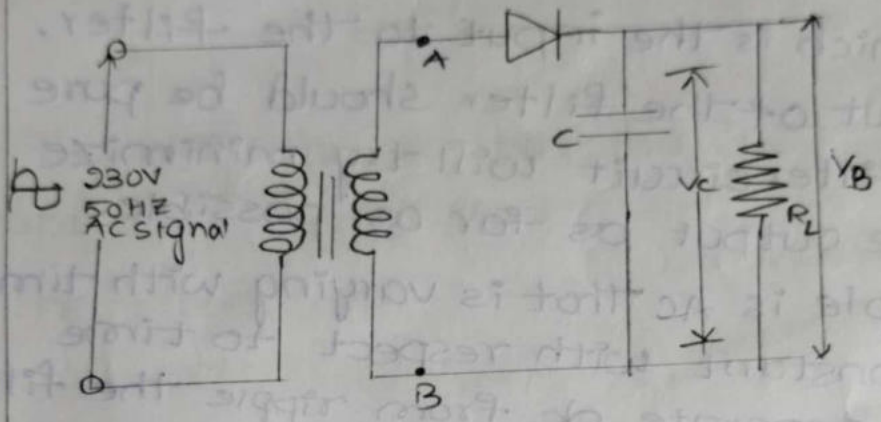
Comparision of rectifiers:-

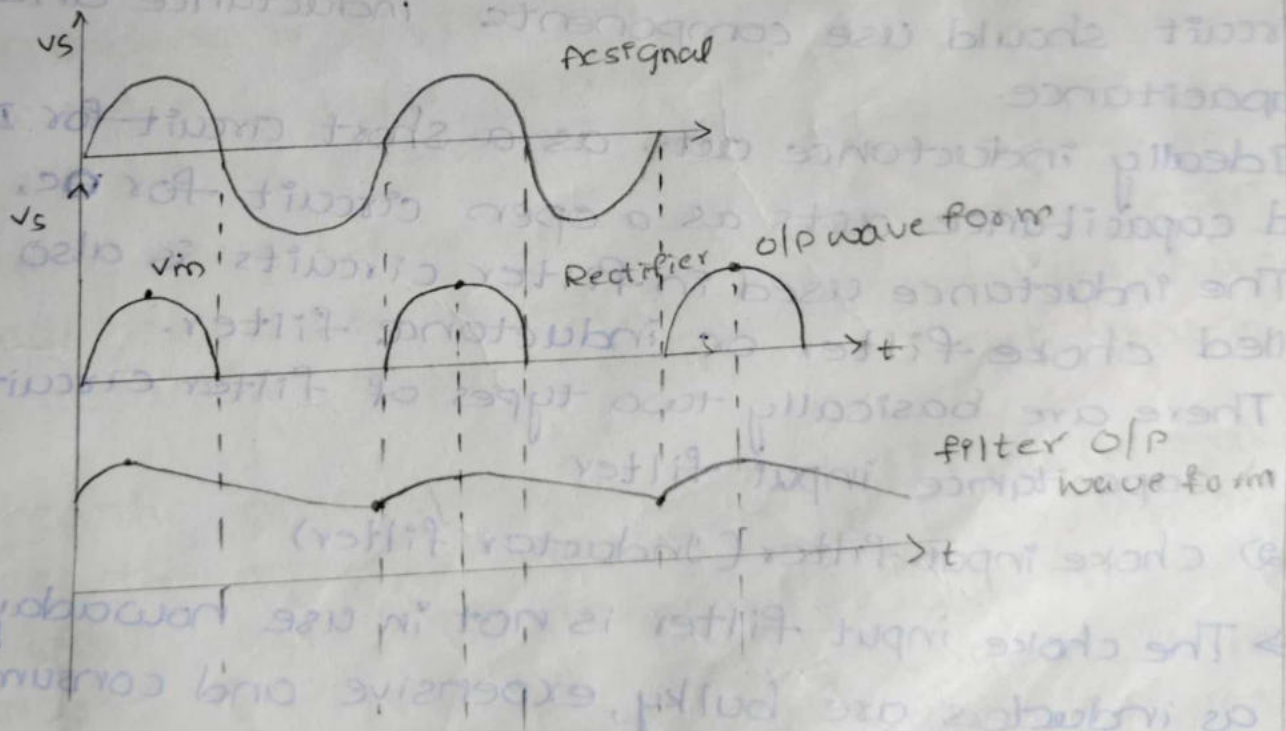
Particular / Parameter	Half wave rectifier	center trapped full wave rectifier	Bridge full wave rectifier
1. Number of diodes	1	2	4
2. Necessity of center tapped transformer.	Not necessary	Neccessary	Not necessary
3. Maximum efficiency.	40.6%	81.1 or 2%	81.1 or 2 %.
4. Ripple factor.	1.21	0.48	0.48
5. Output frequency (ripple frequency).	Same as input	twice the input	twice the input
6. Peak inverse voltage	Vm	2Vm	Vm

Filters :-

Capacitance filter :-







Filters circuits:-

→ It is seen that the output of half wave or full wave rectifier circuit, is not pure dc but it contains fluctuations or ripples which are undesi

→ To minimize the ripple content in the output fil circuits are used. These circuits are connected b the rectifier and load as shown in fig above

→ As an ac input is applied to the rectifier at the output of the rectifier there will be dc and ripp voltage present which is the input to the filter.

→ Ideally the output of the filter should be pure practically the filter circuit will try minimize the ripple at the output as far as possible.

→ Basically the ripple is AC that is varying with tim while Dc is a constant with respect to time hence, in order to seperate dc from ripple the fil circuit should use components inductance and capacitance.

→ Ideally inductance acts as a short circuit for DC and capacitance acts as a open circuit for Dc.

→ The inductance used in filter circuits is also called choke filter or inductance filter.

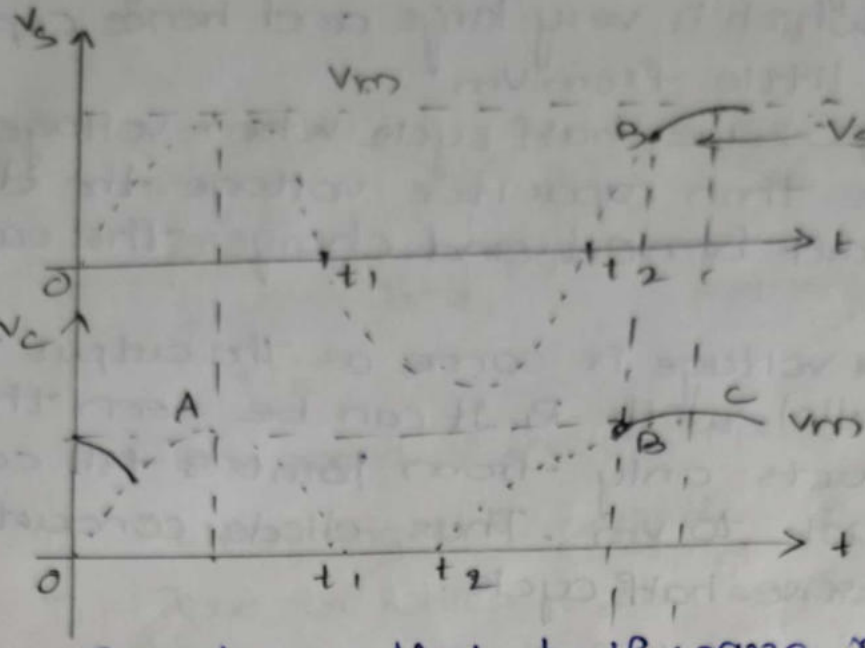
There are basically two types of filter circuits

1) capacitance input filter

2) choke input filter (Inductor filter)

→ The choke input filter is not in use nowaday as inductors are bulky, expensive and consume more power.

Capacitor input filter or Series Shunt capacitance filter:



→ The fig shows that half wave rectifier with capacitor input filter.

→ The filter uses a single capacitor connected in parallel with the load represented by the resistance R_L.

→ In order to minimize the ripples in the output the capacitor 'c' is used in the filter circuit is quite large of the order of tens of microfarads.

→ During the positive quarter cycle of the input signal the diode is forward biased this charges the capacitor to peak value of input that is V_m.

→ When the input starts decreasing below its peak value the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.

→ So, during the entire negative half cycle and some part of positive half cycle, capacitor discharges through R_L.

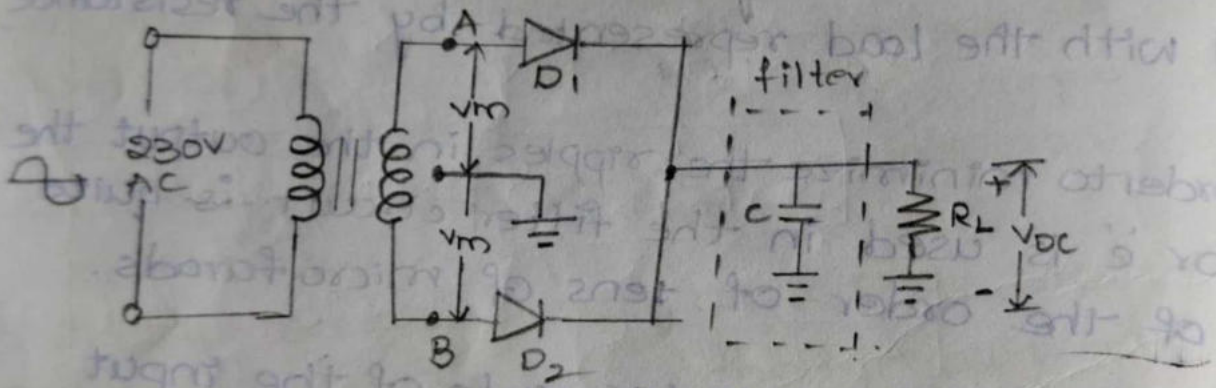
→ The discharging of capacitor is decided by $R_L C$ time constant which is very large and hence capacitor discharges very little from V_m.

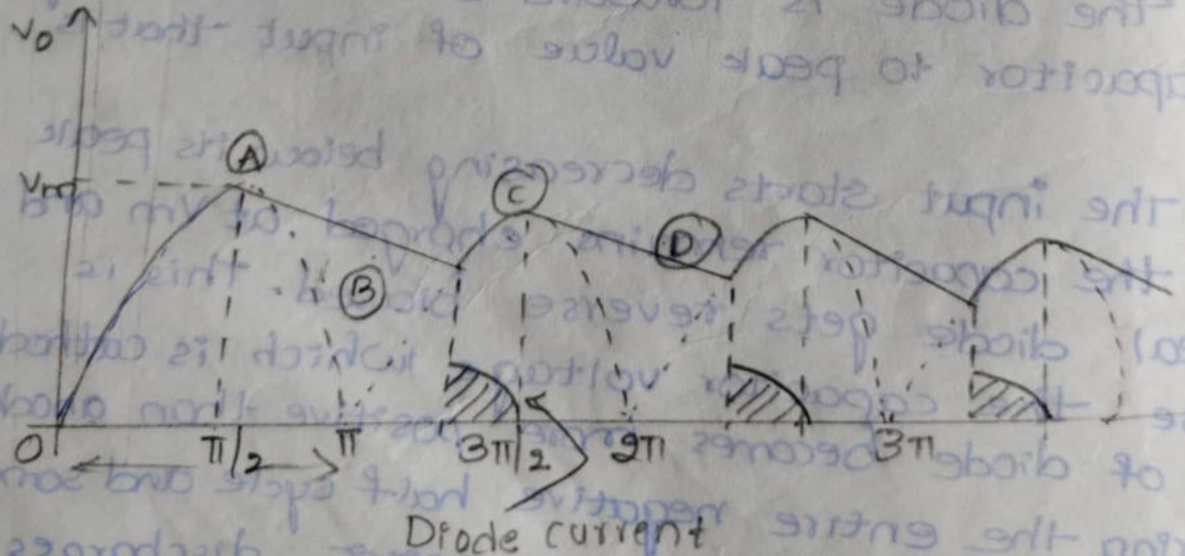
→ In the next positive half cycle when voltage source V_s becomes more than capacitor voltage the diode becomes forward biased and charges the capacitor back to V_m.

→ The capacitor voltage is same as the output voltage as it is in parallel with R_L. It can be seen that the diode conducts only from point B till capacitor gets charged back to V_m. Thus, diode conducts only for part of positive half cycle.

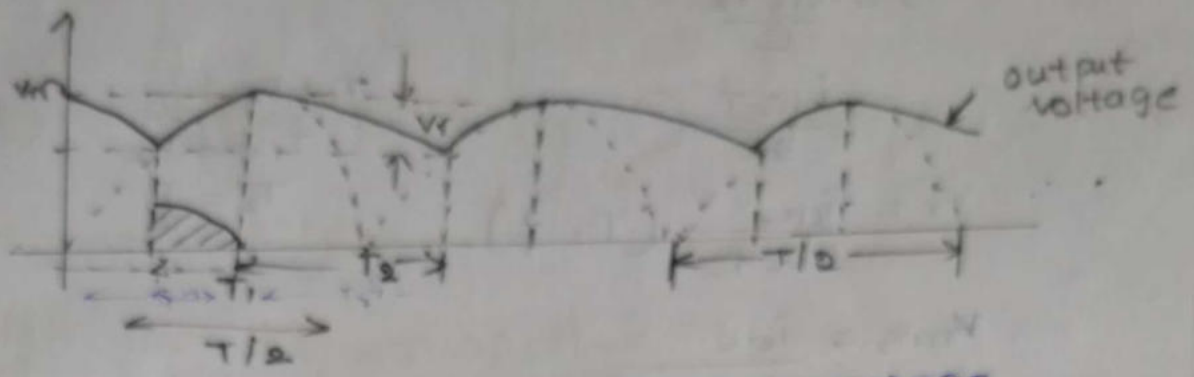
→ From point A to B the diode remains non conducting and conducts only for the period from B to C.

Full wave rectifier with capacitor filter:-





Expression for ripple factor :-



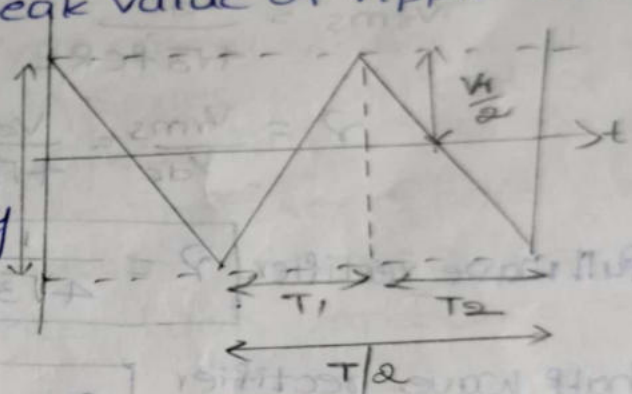
T = Time period of the ac input voltage

T/2 = Half of the time period

T_1 = Time for which diode is conducting

T_2 = Time for which diode is non conducting

Let V_r be the peak to peak value of ripple voltage which is assumed to be triangular as shown in fig.



→ It is known mathematically that the rms value of such a triangular wave form,

$$V_{rms} = \frac{V_r}{2\sqrt{3}} \rightarrow (1)$$

→ During the time interval t_2, the capacitor 'c' is discharging through the load resistance R_L. The charge lost is

$$Q = CV_r \rightarrow (2)$$

$$i = \frac{dQ}{dt}$$

$$Q = \int_0^{t_2} i\, dt$$

$$Q = i_{dc}\,[t]_0^{T_2}$$

$$Q = i_{dc}\, T_2 \rightarrow (3)$$

$C \cdot V_r = i_{dc} T_2$

$V_r = \frac{i_{dc} T_2}{C}$

$= \frac{i_{dc} T}{2C}$

$T_1 + T_2 = \frac{T}{2}$

$T_1 << T_2$

$T_2 = \frac{T}{2}$

$V_r = \frac{i_{dc} \times 1}{2Cf} \quad (T = \frac{1}{f})$

$V_{rms} = \frac{i_{dc}}{2fC \times 2\sqrt{3}}$

$V_{rms} = \frac{i_{dc}}{4\sqrt{3} fC}$

We know, $\boxed{i_{dc} = \frac{V_{dc}}{R_L}}$

$V_{rms} = \frac{V_{dc}}{4\sqrt{3} fCR_L}$

$\gamma = \frac{V_{rms}}{V_{dc}} = \frac{V_{dc}}{4\sqrt{3} fCR_L V_{dc}}$

For full wave rectifier $\boxed{\gamma = \frac{1}{4\sqrt{3} fCR_L}}$

For half wave rectifier $\boxed{\gamma = \frac{1}{2\sqrt{3} fCR_L}}$

→ From the expression of the ripple factor it is clear that increasing the value of the capacitor 'c' the ripple factor gets decreased.

→ Thus, the output can be made smoother reducing the ripple content by selecting large value of capacitor

Inductor filter or choke filter :-

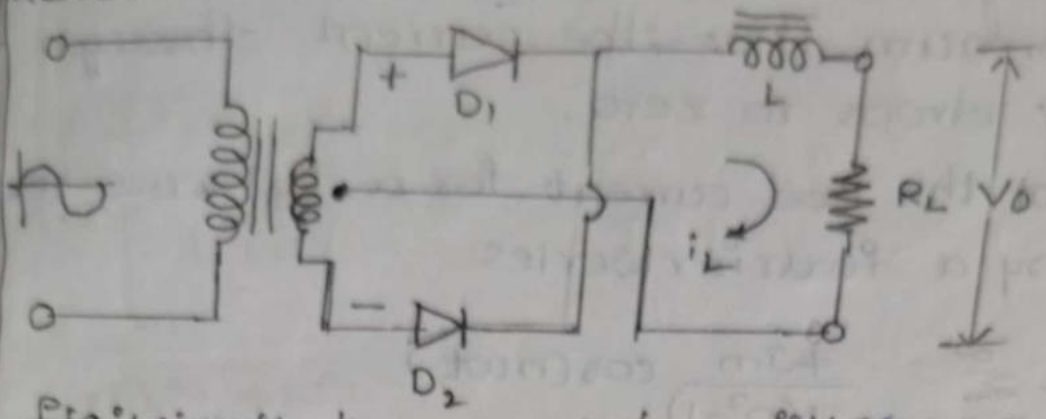


fig: circuit diagram of choke filter

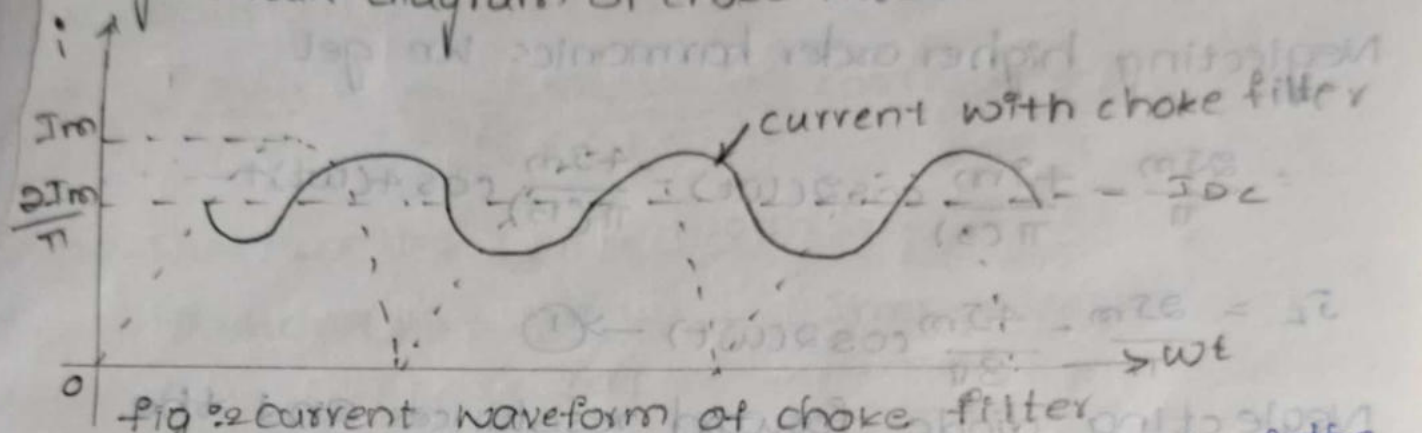


fig: current waveform of choke filter

→ An inductor is connected in series with load of the rectifier it is also called as choke filter. The fundamental property of an inductor is that to oppose any changes in the current passing through it. Thus an inductor presence high impedance to ac and none to DC.

→ The inductor stores energy in it as magnetic field when the current is above its average value and delivers that energy to the circuit, when the current tends to fall below the average value.

→ Thus, it reduces the pulsation of the rectifier output.

→ As shown in fig 2 when output tends to size above the average value magnetic energy is stored in the inductor which has the effect of toning down smothening the sudden raise in current. However, when current tends to fall below the average value, this stored energy is returned to circuit

→ In this way the current variations are reduced to the minimum. Thus the current through the load never drops to zero.

We know that the load current for a full wave rectifier is given by a fourier series

$$I_L = \frac{4I_m}{2\pi} - \sum_{n=2,4,6\ldots}^{\infty} \frac{4I_m}{\pi(n^2-1)} \cos(n\omega t)$$

Neglecting higher order harmonics we get

$$= \frac{2I_m}{\pi} - \frac{4I_m}{\pi(3)} \cos 2(\omega t) - \frac{4I_m}{\pi(15)} \cos 4(\omega t) + \ldots$$

$$I_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2(\omega t) \rightarrow (1)$$

Neglecting diode forward resistances and the resistance of choke and transformer secondary, we can write the dc component of current as

$$I_{dc} = \frac{2I_m}{\pi}$$

$$I_m = \frac{V_m}{R_L + R_f + R_s}$$

$$R_f + R_s \ll R_s$$

$$I_m = \frac{V_m}{R_L}$$

$$\boxed{I_{dc} = \frac{2V_m}{\pi R_L}}$$

→ While the second harmonic component represents ac components or ripple presence can be written as

$$I_m = \frac{V_m}{Z}$$

$$Z = R_L + j2X_L$$

$X_L = 2\pi f L$

$X_L = \omega L$

$Z = \sqrt{R_L^2 + (2X_L)^2}$

$\phi = \tan^{-1}\left(\frac{2X_L}{R_L}\right)$

$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}$

Hence equation ① modified as

$$I_L = \frac{2V_m}{\pi R_L} - \frac{4}{3\pi} \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \cos(2\omega t - \phi)$$

Expression for the ripple factor :-

Ripple factor (γ) = $\frac{V_{rms}}{V_{dc}}$ or $\frac{I_{rms}}{I_{dc}}$

$V_{rms} = \frac{V_m}{\sqrt{2}}$ $\quad I_{rms} = \frac{I_m}{\sqrt{2}}$

$$\gamma = \frac{\frac{4V_m}{\sqrt{2}\,3\pi\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}}$$

$$\gamma = \frac{4}{3\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}} \times \frac{R_L}{2}$$

$$\gamma = \frac{2R_L}{3\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$\gamma = \frac{2R_L}{3\sqrt{2}R_L\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

$$\gamma = \frac{2}{3\sqrt{2}\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

Initially, on no load condition $R_L \to \infty$ and hence $\frac{4\omega^2 L^2}{R_L^2} \to 0$ $\quad \gamma = \frac{2}{3\sqrt{2}\sqrt{1}}$ $\quad \gamma = 0.472 \Rightarrow 47.1\%$

→ This is very close to normal full wave rectifier without filtering.

→ But as load increases, R_L decreases hence $\frac{4\omega^2 L^2}{R_L^2} >> 1$ so neglecting one we get,

$$= \frac{2}{3\sqrt{2}\sqrt{\frac{4\omega^2 L^2}{R_L^2}}} = \frac{2}{3\sqrt{2}\frac{2\omega L}{R_L}}$$

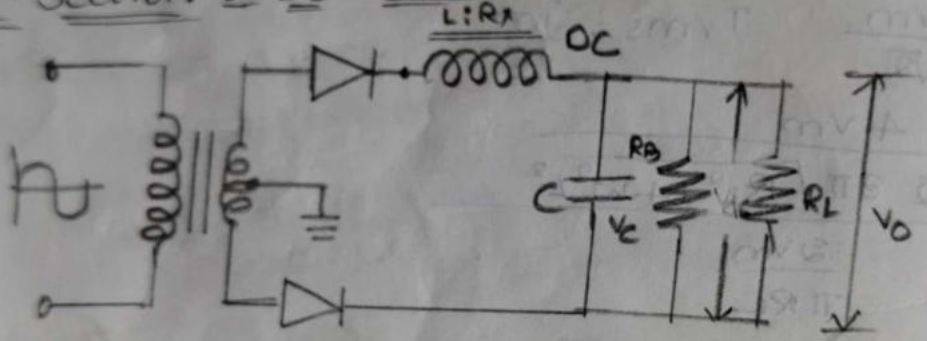
$$= \frac{R_L}{3\sqrt{2}\omega L}$$

$$= \frac{\sqrt{2}R_L}{3\,2\omega L}$$

$$= \frac{R_L}{3\sqrt{2}\omega L}$$

→ So as load changes, ripple changes which is inversely proportional to the value of the inductor.

L-Section or LC filter:-



L : short-DC
open-AC

C : short AC
open DC

→ The dc winding resistance of the choke is R_x. The circuit is also called L-type filter or LC filter. The basic requirement of this filter circuit is that the current through choke must be continuous and not interupted.

→ An interupted current through choke may develop a large back emf which may be in excess of PIV rating of the diodes and maximum voltage rating of capacitor C.

→ Thus, this back emf is harmful to the diodes and capacitor. To eleminate the back emf developed across the choke, the current through it must be maintained continuous.

This is assumed by connecting a bleeder resistance R_B across the output terminals.

Bleeder resistance:-

In electronics a bleeder resistor is a safety discharged resistor. It is a resistor connected in parallel with output of high voltage power supply circuit for the purpose of discharging the electric charge stored in the power supplies.

Expression for ripple factor:-

We know that the load current for a full wave rectifier is given by fourier series

$$I_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos(2\omega t)$$

$$I_{dc} = \frac{2I_m}{\pi}$$

$$I_m = \frac{V_m}{R_x + R}$$

$$R = R_B \| R_L$$

$$\boxed{R = \frac{R_B \cdot R_L}{R_B + R_L}}$$

$$I_{dc} = \frac{2 V_m}{\pi (R_x + R)}$$

$$V_{dc} = I_{dc} \times R$$

$$= \frac{2 V_m}{\pi (R_x + R)} \times R$$

$$= \frac{2 V_m}{\pi R} \times R \quad (\because R_x << R)$$

$$\boxed{V_{dc} = \frac{2 V_m}{\pi}}$$

$$I_{ac} = \frac{V_{ac}}{Z}$$

$$I_{ac} = \frac{V_{ac}}{X_L + X_C}$$

$$I_{ac} = \frac{4 V_m}{3\pi (X_L + X_C)}$$

$$I_{ac} = \frac{4 V_m}{3\pi X_C \left(\frac{X_L}{X_C} + 1\right)}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \text{or} \quad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$I_{ac} = \frac{4 V_m}{3\sqrt{2}\pi X_C \left(\frac{X_L}{X_C} + 1\right)}$$

$$V_{rms} = I_{rms} \times X_C$$

$$= \frac{4 V_m}{3\sqrt{2}\pi X_C \left(1 + \frac{X_L}{X_C}\right)} \times X_C$$

$$\boxed{V_{rms} = \frac{4 V_m}{3\sqrt{2}\pi \left(1 + \frac{X_L}{X_C}\right)}}$$

$$\rho = \frac{V_{rms}}{V_{dc}}$$

$$\rho = \frac{\frac{4 V_m}{3\sqrt{2}\pi \left(1 + \frac{X_L}{X_C}\right)}}{\frac{2 V_m}{\pi}} = \frac{2}{3\sqrt{2}\left(1 + \frac{X_L}{X_C}\right)} = \frac{2}{3\sqrt{2}\left(\frac{X_L}{X_C}\right)}$$

$$\frac{X_L}{X_C} >> 1$$

$X_L = 2\omega L$; $X_C = \frac{1}{2\omega C}$

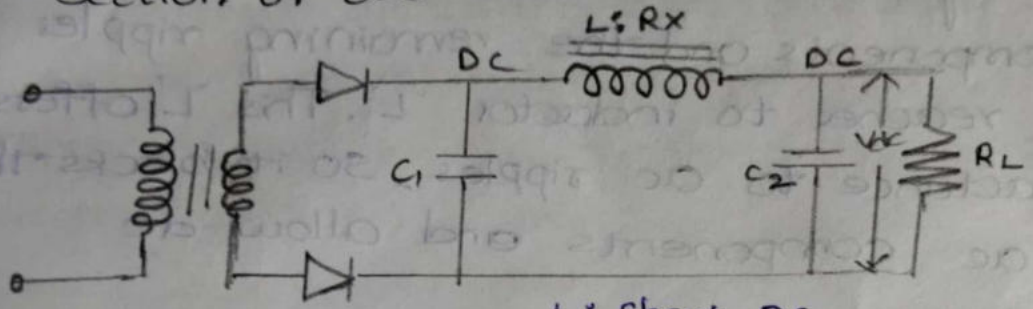
$$\gamma = \frac{2X_C}{3\sqrt{2}X_L}$$

$$\gamma = \frac{2}{3\sqrt{2}} \times \frac{1}{2\omega L \times 2\omega C}$$

$$\boxed{\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}}$$

→ It is seen that ripple factor for choke L-section filter does not depend upon the load resistance unlike the capacitor input filter.

π - Section or CLC filter :-



L : Short DC
Open AC

C : Short AC
open DC

$$\gamma_{\pi\text{.section}} = \gamma_{\text{capacitor}} \cdot \gamma_{\text{L-section}}$$

$$= \frac{1}{4\sqrt{3}fC_1R_L} \times \frac{1}{6\sqrt{2}\omega^2 LC_2}$$

$$= \frac{\pi}{2\sqrt{3}\,2\pi f C_1 R_L} \times \frac{1}{6\sqrt{2}\omega^2 LC_2}$$

$$\simeq \frac{\pi}{2\sqrt{3}\,\omega C_1 R_L} \times \frac{1}{6\sqrt{2}\omega^2 LC_2}$$

$$= \frac{\pi}{12\sqrt{6}\omega^3 C_1 C_2 R_L \cdot L}$$

$$= \frac{0.106}{\omega^3 C_1 C_2 L R_L}$$

→ It consists of Inductor L and two capacitors C_1 & C_2 these components are arranged in the form greek

letter 'π', hence the name π-section filters
a shunt capacitor filter is added to L-section filter to from the π-section filter.

→ The π-section filter provides an output voltage that approaches the peak value of the dc potential of the supply, the ripple components being very small.

→ As we discussed in the previous section, the rectified output is given to the filter in this case that is to the capacitor C_1 followed by L-section (LC 2) the capacitor C_1 offers very low reactance to the ripples and by passes most of them.

→ The DC components and the remaining ripples then reaches to inductor 'L'. This 'L' offers very high reactance to ac ripples, so it blocks the maximum ac components and allow dc components.

→ The remaining small amount ac ripples and dc then reaches to the capacitor C_2 and it by passes almost all the ripple and supplies almost pure dc to the load R_L.

→ Thus, π-section filter produces a unidirectional output voltage across the load R_L with negligible ripples.

Clipper circuits are limiters:-

→ The basic action of clipper circuit is to remove the certain portion of the wave form above or below the certain level as per the requirements.

→ The circuits which are used to clip off unwanted portion of the wave form, without distorting the remaining part of the wave form are called clipper circuits or clippers.

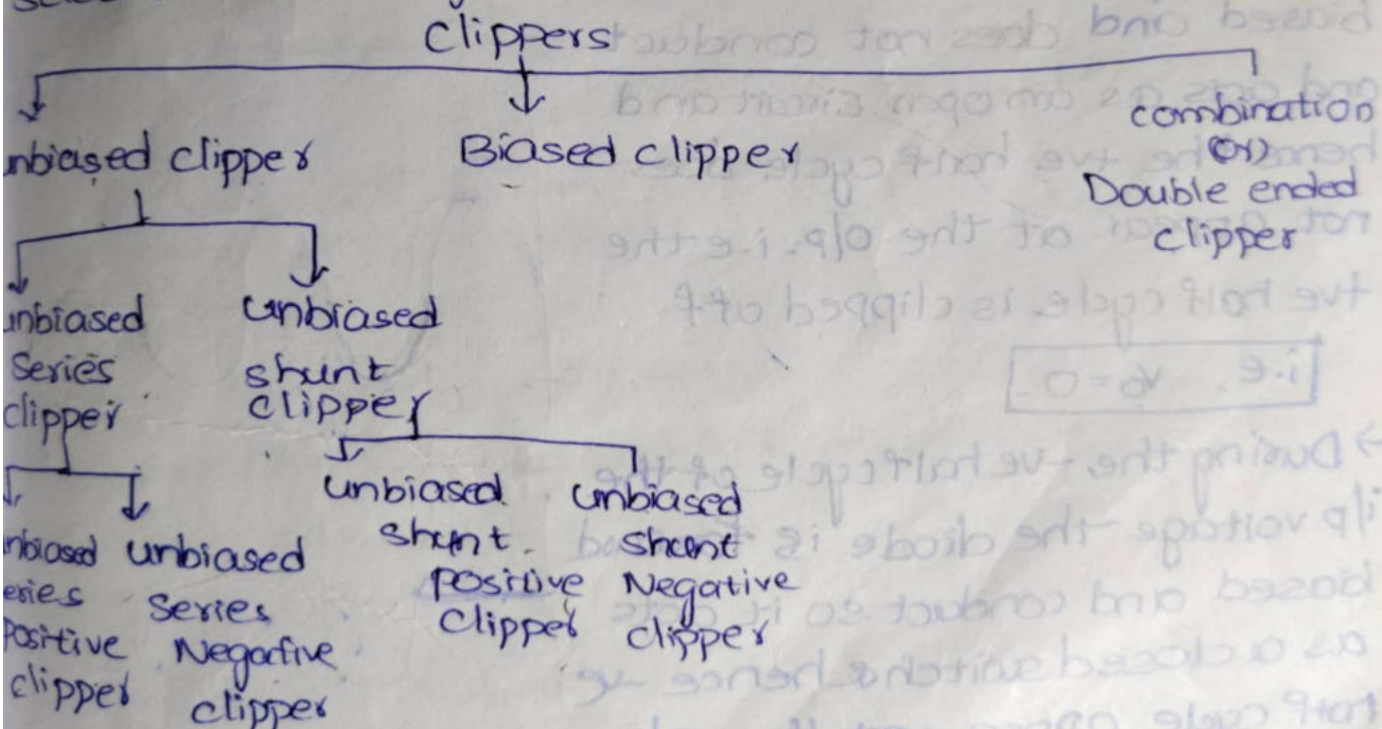
⇒ The half wave rectifier is the best and simplest type of clipper circuit which clips off the negative portion of input signal by changing the orientation of the diode in the circuit positive or negative portion of input signal can be clipped off.

⇒ The clipper circuits are also called limiters or slicers.

⇒ The clipper circuits are mainly classified depending upon the orientation of the diode in the circuit.

Clippers:- The circuit which removes a portion of input signal without distorting the remaining part of the input waveform is called clipper.

⇒ Clipper circuits are also reffered to as amplitude selector (or) voltage limiter



Biased clipper

- Biased series clipper
  - Biased series +ve clipper with +ve reference
  - Biased series +ve with -ve reference
  - Biased series -ve with +ve reference
  - Biased series -ve with -ve reference
- Biased shunt clipper
  - Biased shunt +ve clipper with +ve reference
  - Biased shunt +ve with -ve reference
  - Biased shunt -ve with +ve reference
  - Biased shunt -ve with -ve reference

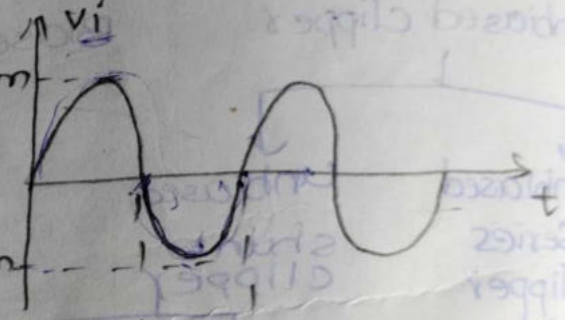
Unbiased clippers:-

unbiased +ve clippers:-

1) unbiased series diode +ve clipper:-

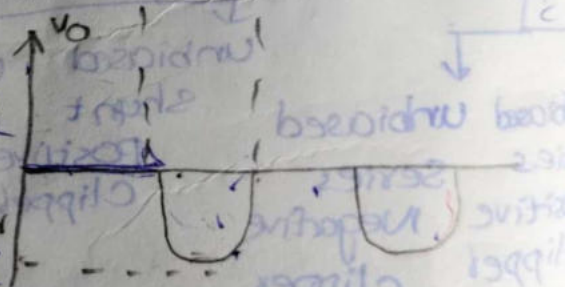
→ During the +ve half cycle of the i/p voltage, the diode is reverse biased and does not conduct and acts as an open circuit and hence the +ve half cycle does not appear at the o/p. i.e the +ve half cycle is clipped off

i.e, $V_o = 0$



→ During the -ve half cycle of the i/p voltage the diode is forward biased and conduct so it acts as a closed switch & hence -ve half cycle appears at the o/p.

$V_o = V_i$

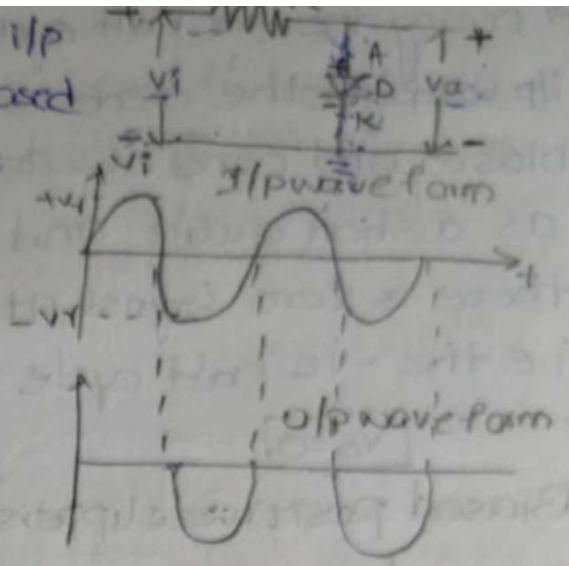


2) unbiased shunt diode +ve clipper:-

→ During the +ve half cycle of the i/p voltage diode is Fw biased and conducts and acts as short ckt and hence there is zero signal at the o/p. i.e +ve half cycle is clipped off. $V_o = 0$

→ During the -ve half cycle of the i/p voltage, the diode is reverse biased and does not conduct and acts as an open switch and hence negative half cycle appears at the o/p

$V_o = V_i$

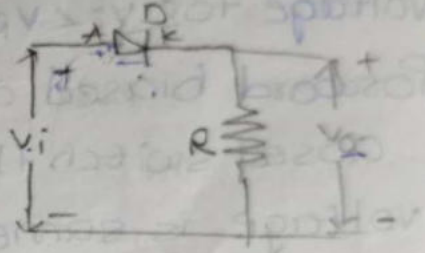


Unbiased -ve clippers:-

Series diode -ve clipper:-

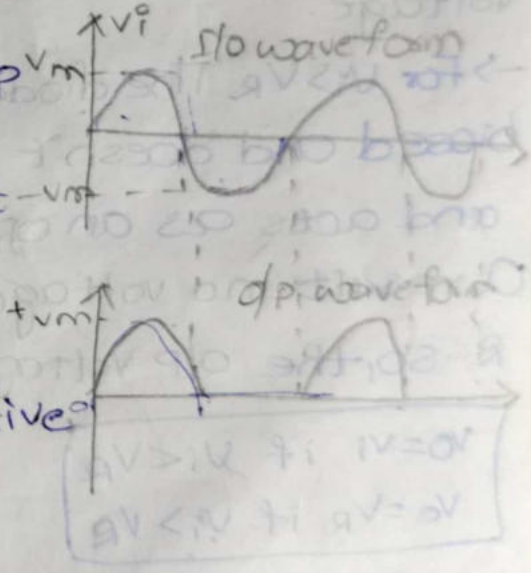
→ During the +ve half cycle of i/p voltage the diode is f.w biased and conducts so it acts as closed switch & hence +ve half cycle appears at the o/p.

$V_o = V_i$



→ During the -ve half cycle of the i/p voltage the diode is reverse biased and doesn't conducts. so it acts as open switch and hence negative half cycle will not appear at the o/p i.e the negative half cycle is clipped off.

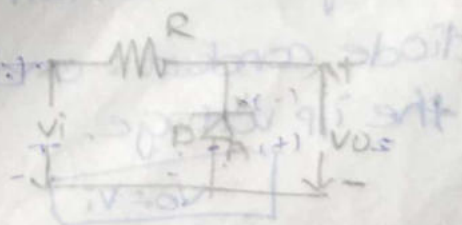
$V_o = 0$



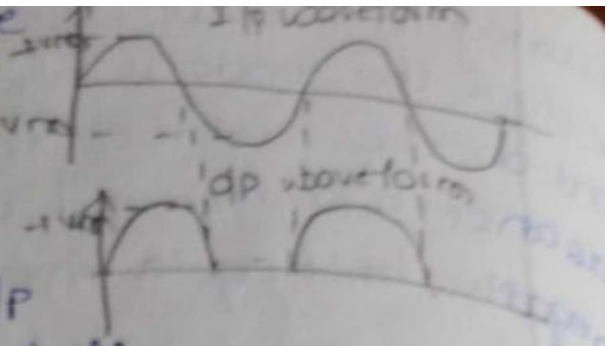
Shunt diode -ve clipper:-

→ During the +ve half cycle of the i/p voltage, the diode is reverse biased and doesn't conduct and acts as an open ckt. so, the +ve half cycle of the i/p voltage appears as the o/p.

$V_o = V_i$



→ During the -ve half cycle of the i/p voltage, the diode is forward biased and conducts and acts as a short circuit and hence there is zero signal at the o/p i.e the -ve half cycle is clipped off

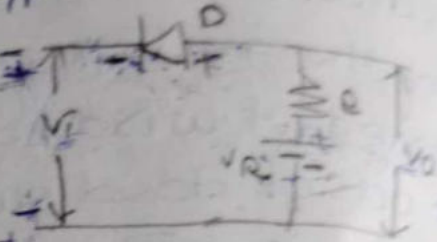


$V_o = 0$

Biased positive clippers:-

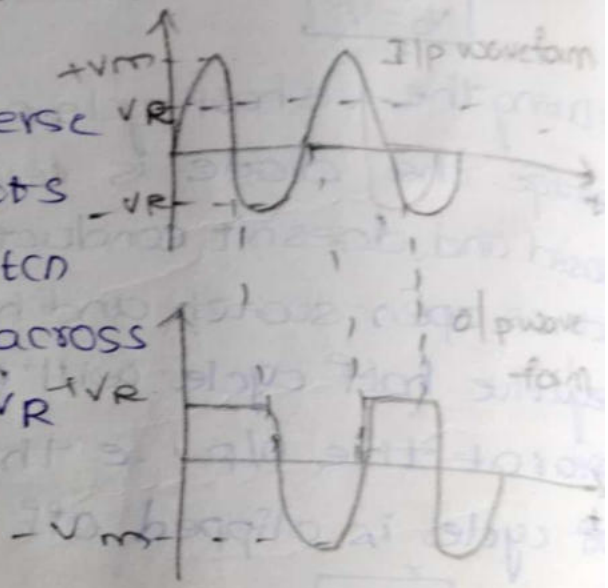
Series diode positive clipper:- with +ve reference

→ During the +ve halfcycle of the i/p voltage for $V_i < V_R$ the diode is forward biased and acts as a closed switch hence the o/p voltage is same as the i/p voltage.



→ For $V_i > V_R$ The diode is reverse biased and doesn't conducts and acts as an open switch

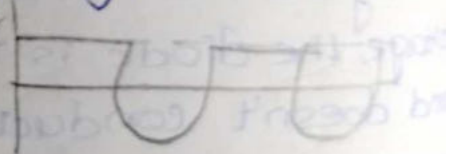
A result no voltage drop across R. So, the o/p voltage $V_o = V_R + V_R$



$V_o = V_i$ if $V_i < V_R$

$V_o = V_R$ if $V_i > V_R$

During the -ve half cycle of the i/p voltage, the diode conducts and hence o/p voltage is same as the i/p voltage.



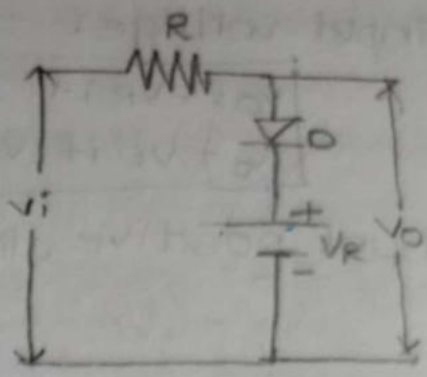
$V_o = V_i$

Shunt diode positive clipper with +ve reference:-

→ During the +ve half cycle of the i/p voltage for $V_i < V_R$ the diode is reverse biased and doesn't conducts and acts as open switch hence the o/p voltage

same as the i/p voltage.

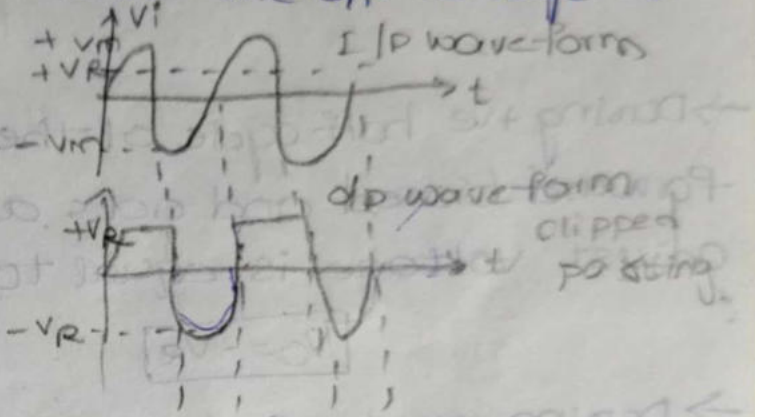
for $V_i > V_R$ the diode is forward biased and conducts and output remains at V_R until the V_i becomes less than V_R



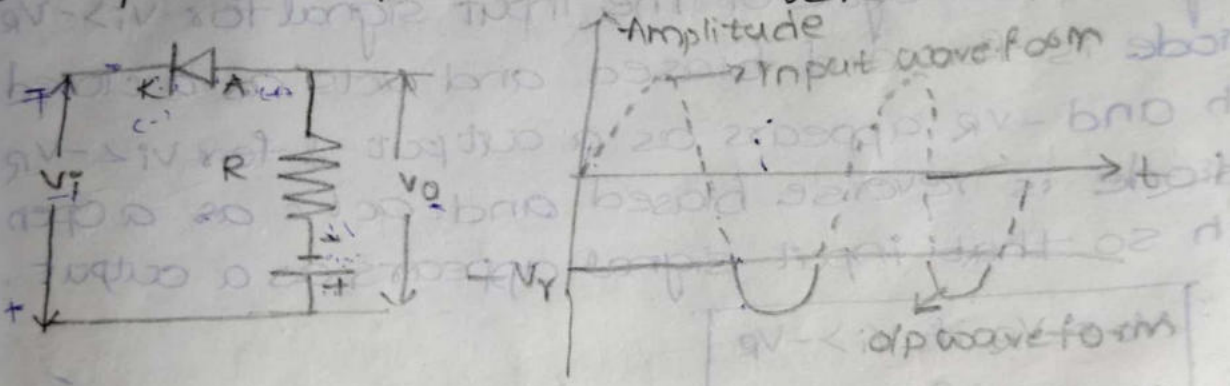
$V_o = V_R$ if $V_i > V_R$
$V_o = V_i$ if $V_i < V_R$

During the -ve half cycle of the i/p voltage the diode is reverse biased and does not conducts and acts as open switch and hence the o/p voltage is same as the i/p voltage.

$V_o = V_i$



Series positive clippers with -ve reference:-



→ During +ve half cycle of the i/p signal the diode is reverse biased and acts as an open switch as a result no voltage appears across load resistor and output voltage V_o is equal to $-V_R$

$V_o = -V_R$

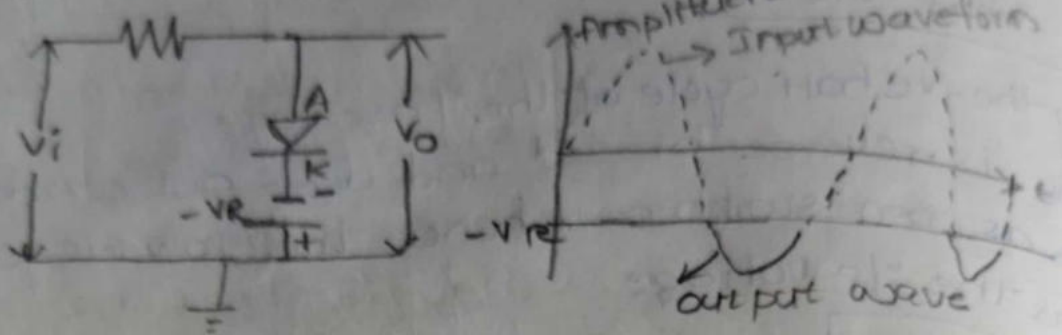
→ During -ve half cycle of the i/p signal for $V_i > -V_R$ the diode is reverse biased and doesn't conducts and output voltage is equivalent to $-V_R$ and for $V_i < -V_R$ the diode is forward biased and acts as a

closed switch so that output voltage is same as input voltage.

$V_o = -V_R$ if $V_i > -V_R$

$V_o = V_i$ if $V_i < -V_R$

Shunt positive clipper with -ve reference



→ During +ve half cycle of the input signal the diode is forward biased and acts as a closed switch so, that adjust voltage is equal to reference voltage

$V_o = -V_R$

→ During -ve half cycle of the input signal for $V_i > -V_R$ the diode is forward biased and acts as a closed switch and $-V_R$ appears as a output & for $V_i < -V_R$ the diode is reverse biased and acts as a open switch so that input signal appears as a output

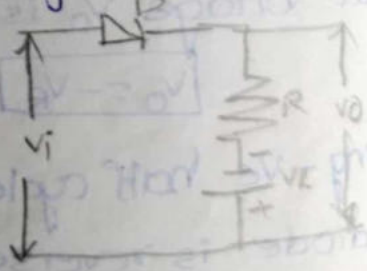
$V_o = -V_R$ if $V_i > -V_R$

$V_o = V_i$ if $V_i < -V_R$

Biased Negative clippers:-

Series diode negative clipper with -ve reference:

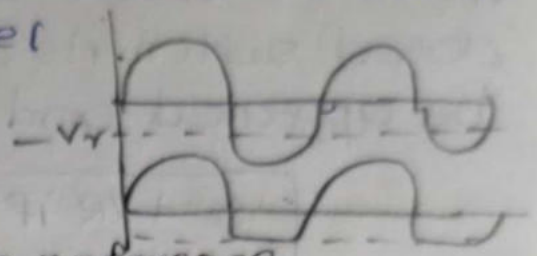
→ During the +ve half cycle of the i/p voltage the diode is forward biased and conducts and hence o/p voltage is same as the i/p voltage



$V_o = V_i$

During the -ve half cycle of the i/p voltage for $V_i > V_R$ the diode is forward biased and acts as a closed switch. Hence the o/p voltage is same as the i/p voltage. For $V_i < -V_R$ the diode doesnot conduct so the o/p voltage is at $-V_R$ level

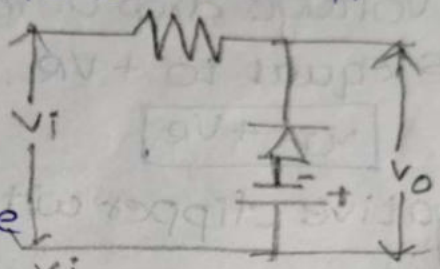
$V_o = V_i$ for $V_i > -V_R$
$V_o = -V_R$ for $V_i < -V_R$



Shunt diode Negative clipper with -ve reference

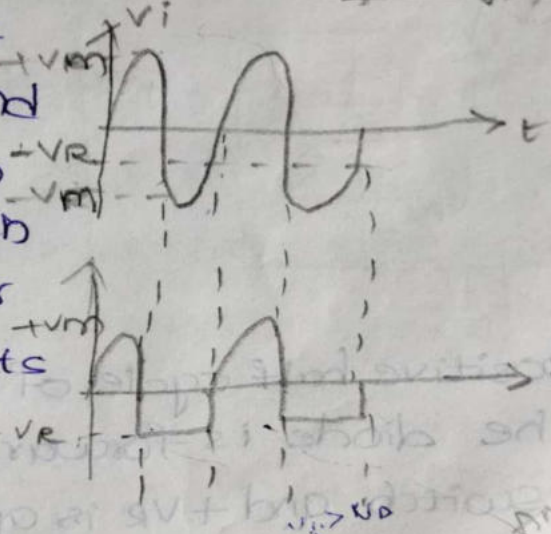
During the +ve half cycle of the i/p voltage the diode is reverse biased and doesn't conducts and acts as open switch and hence the o/p is same as i/p voltage

$V_o = V_i$

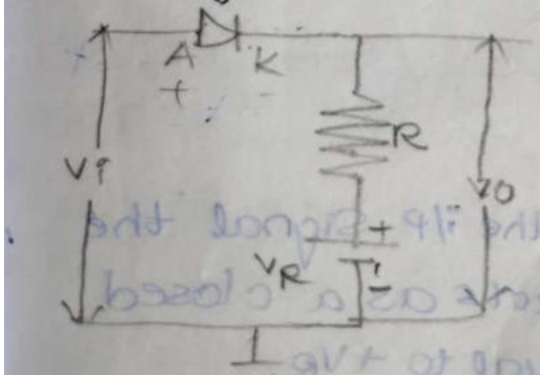


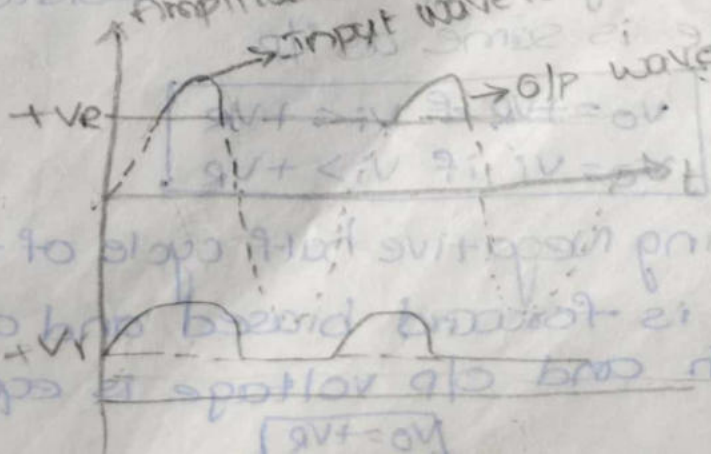
During the -ve half cycle of the i/p voltage for $V_i > -V_R$ the diode doesn't conduct and it acts as an open switch so, the o/p voltage switch is same as i/p voltage. For $V_i < -V_R$ the diode conducts and at $-V_R$ level.

$V_o = V_i$ for $V_i > -V_R$
$V_o = -V_R$ for $V_i < -V_R$



Series Negative clipper with +ve reference:-





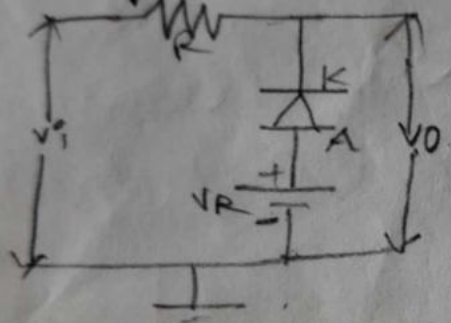
→ During +ve half cycle of the i/p signal for $V_i \leq V_R$ the diode is reverse biased and acts as a open switch so that output voltage is equal to $+V_R$ and for $V_i > V_R$ the diode is forward biased and acts as closed switch. As a result voltage drop across R will be appeared and output voltage $V_o = V_i$

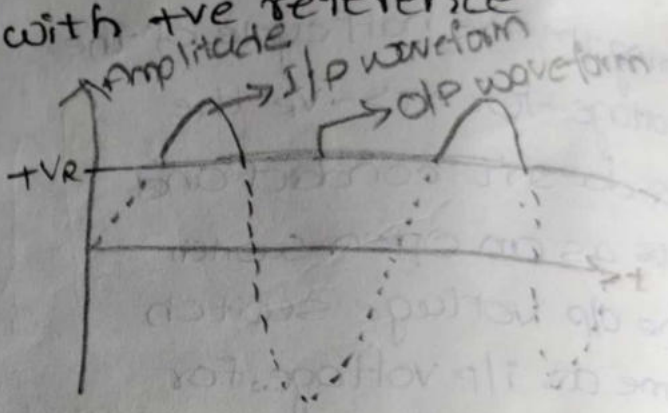
$$V_o = +V_R \text{ if } V_i < V_R$$
$$V_o = V_i \text{ if } V_i > V_R$$

→ During -ve half cycle of the i/p signal the diode is reverse biased and acts as a open switch as a result no voltage drop across Resistor R. So, the output voltage is equal to $+V_R$.

$$V_o = +V_R$$

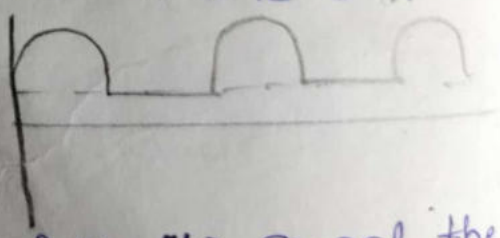
Shunt Negative clipper with +ve reference





→ During positive half cycle of the input signal for $V_i < +V_R$ the diode is forward biased and acts as a closed switch and $+V_R$ is appears as output and for $V_i > +V_R$ the diode is reverse biased and there is a voltage drop across resistor R and output voltage is same as i/p.

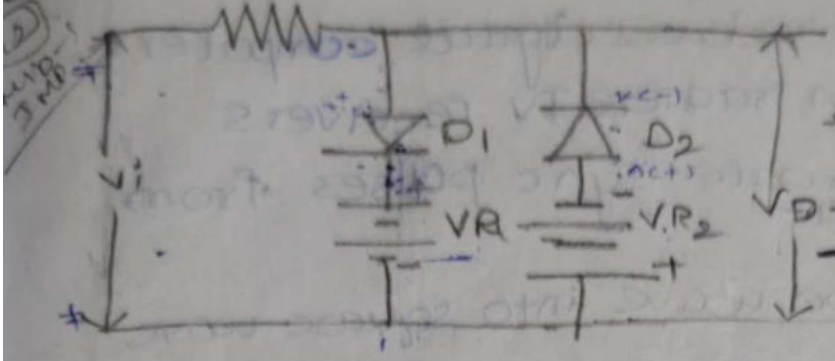
$$V_o = +V_R \text{ if } V_i < +V_R$$
$$V_o = V_i \text{ if } V_i > +V_R$$

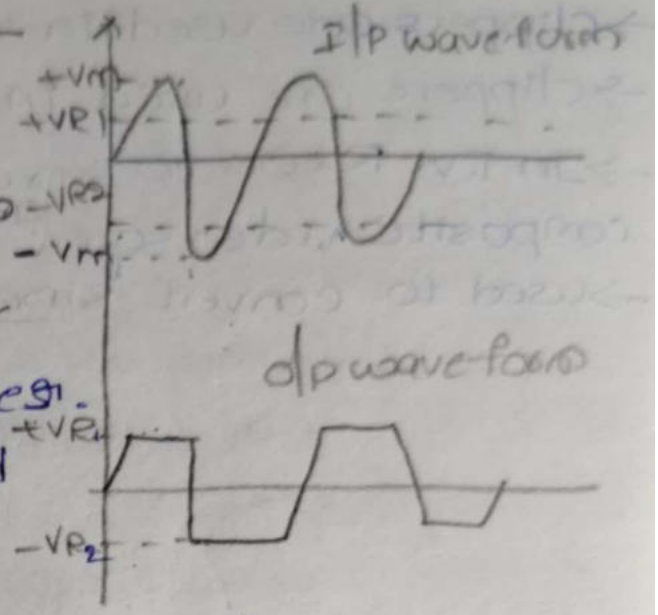


→ During Negative half cycle of the i/p signal the diode is forward biased and acts as a closed switch and o/p voltage is equal to $+V_R$.

$$V_o = +V_R$$

Double ended clipper or Two level clipper:-





It is also known as two level clipper.

It is a combination of a biased +ve clipper & a biased -ve clipper.

During the +ve half cycle of the i/p voltage, the diode D_2 is reverse biased & acts as open switch.

→ The Diode D_1 conducts for $V_i > +VR_1$ and acts as closed switch and o/p voltage is at $+VR_1$ level. If the i/p voltage $V_i < +VR_1$, the diode D_1 doesn't conduct & acts as open switch so, the o/p voltage is same as i/p voltage. Hence, the o/p voltage V_o can't exceed the voltage level at $+VR_1$ during the half cycle.

i) During the -ve half cycle of the i/p voltage, the Diode D_1 is R.B & acts as an open switch

If the i/p voltage $V_i < -VR_2$ the Diode D_2 conducts and acts as closed switch. So, the o/p voltage is at $-VR_2$ level. when the i/p voltage $V_i > -VR_2$ and Diode D_2 doesn't conduct and acts as an open switch. So, the o/p voltage is same as the i/p voltage. Hence, the o/p voltage V_o can't go below the voltage level of $-VR_2$ during the -ve half cycle.

→ The clipping levels may be changed by varying the values of VR_1 & VR_2

Applications of clipper:-

→ Clippers are used in radars & digital computers.
→ clippers are used in radios & Tv receivers
→ In T.v Rxers to separate sync pulses from composite video sgr.
→ used to convert sine wave into square wave.

+ve half cycle

$V_{in} > +V_R \quad V_o = V_{R1}$

$V_{in} < +V_R \quad V_o = V_{in}$

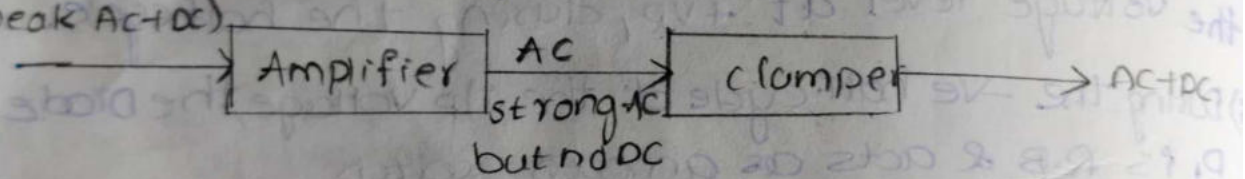
-ve half cycle

$V_{in} > -V_{R2}, \; V_o = V_{in}$

$V_{in} < -V_{R2}, \; V_o = -V_2$

06/06/2023

Clampers: A circuit which adds DC value to an ac waveform without changing its shape. It is used to re-insert dc voltage level into an ac waveform which has lost its dc by passing through the an electronic processing circuit such as amplifier.

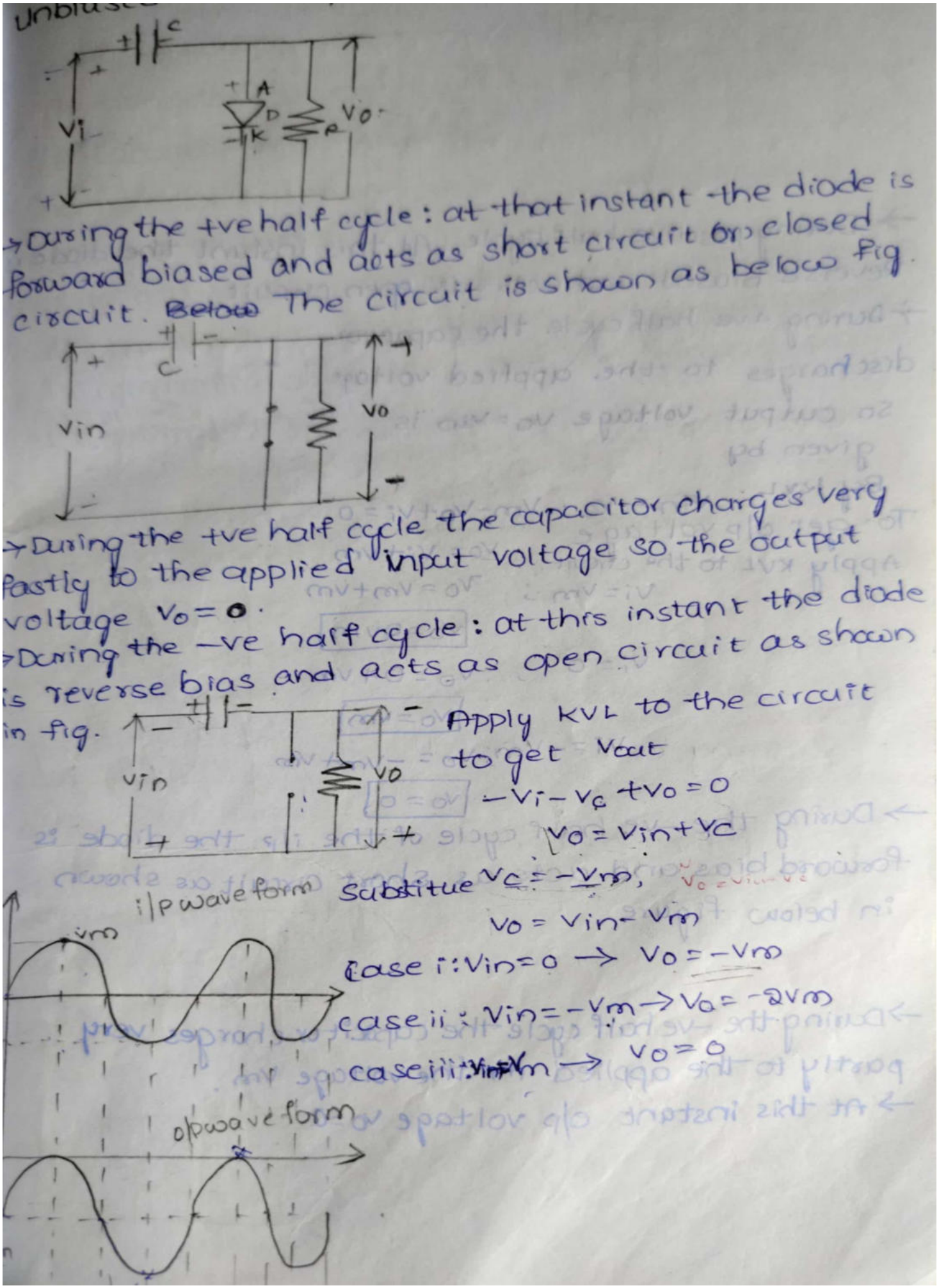


Types of clampers:

1. +ve clamper — Biased, unbiased
2. -ve clamper — Biased, unbiased

+ve clamper: A positive clamper circuit is one that converts a diode, a resistor and a capacitor circuit that shifts the output signal to positive portion of the input signal.

-ve clamper: A Negative clamper circuit is one that converts of a diode, a resistor and a capacitor and that shifts the output signal to negative portion of the input signal



→ During the +ve half cycle: at that instant the diode is forward biased and acts as short circuit or closed circuit. Below The circuit is shown as below fig.

→ During the +ve half cycle the capacitor charges very fastly to the applied input voltage so the output voltage $V_o = 0$.

→ During the −ve half cycle: at this instant the diode is reverse bias and acts as open circuit as shown in fig.

Apply KVL to the circuit to get Vout

$-V_i - V_c + V_o = 0$

$V_o = V_{in} + V_c$

Substitue $V_c = -V_m$,

$V_o = V_{in} - V_m$

i/p waveform

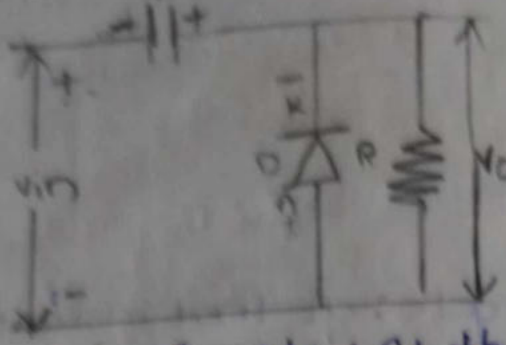
Case i: $V_{in} = 0 \rightarrow V_o = -V_m$

case ii: $V_{in} = -V_m \rightarrow V_o = -2V_m$

case iii: $V_{in} = V_m \rightarrow V_o = 0$

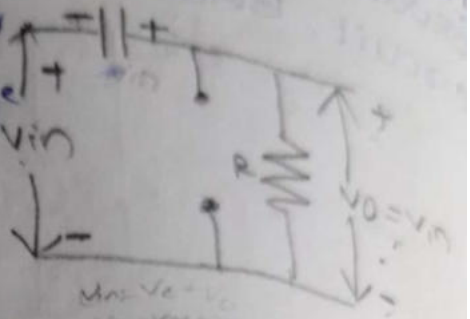
o/p waveform

Unbiased +ve clamper:



→ During positive half cycle: At this instant the diode is Reverse biased and acts as open circuit

→ During +ve half cycle the capacitor discharges to the applied voltage so output voltage $V_o = V_{in}$ is given by



By KVL $-V_m - V_o + V_i = 0$

To get o/p voltage Apply KVL to the circuit:

$$V_o = V_i + V_m$$

$V_i = V_m$; $V_o = V_m + V_m$

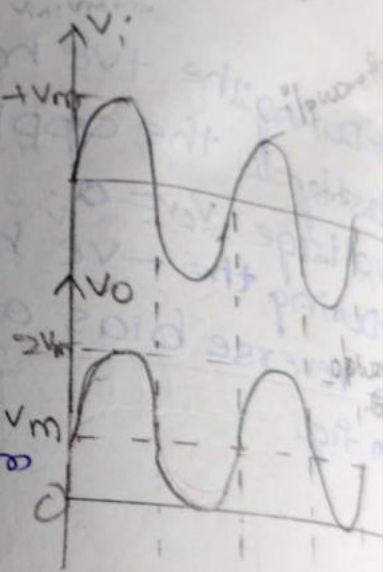
$$V_o = 2V_m$$

$V_i = 0$; $V_o = 0 + V_m$

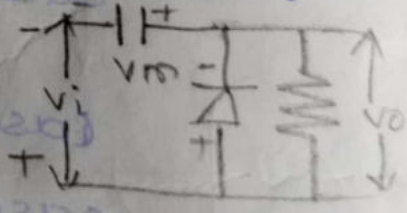
$$V_o = V_m$$

$V_i = -V_m$; $V_o = -V_m + V_m$

$$V_o = 0$$

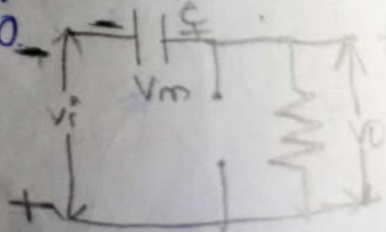


→ During the -ve half cycle of the i/p the diode is forward bias and acts as short circuit as shown in below figure.



→ During the -ve half cycle the capacitor charges very partly to the applied i/p voltage V_m.

→ At this instant o/p voltage $V_o = 0$



Basic Electronics

Electronics is a subject where we study about electrons as well as electronic components. In our universe everything is available in three forms i.e solid, liquid and gas. We can sense them by feeling, touching and can even seeing as well as they have weight, size and there three types conductors insulators and semi conductors.

Conductor:- A conductor is a substance or material that allows electricity to flow through it. In a conductor electrical charge carriers usually electrons or ions move easily from atom to atom when voltage is applied.

Eg:- copper, aluminium, gold, silver etc.

Insulator:- The material that donot allow electricity to pass through them are called insulator.

Eg:- Glass, air, wood, plastic, rubber etc.

Semi conductor:- semi conductors are materials which have a conductivity between conductors and non conductors (Insulator).

Eg:- Silicon, germanium.

Classification of solids on the basis of energy band theory:

Out of all the bands three bands are important to understand the behaviour solids.

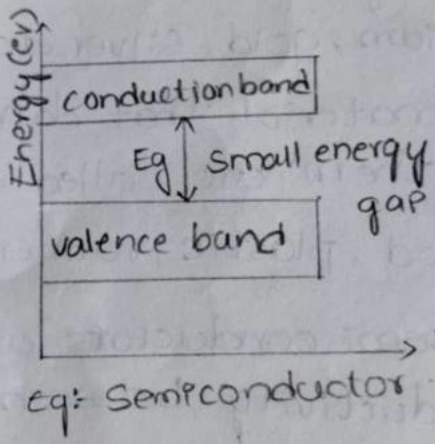
Valence band:- A set of energy level possesed by valence electrons is known as valence band. It is obviously the highest occupied band as regards occupiency it may be either completely

filled or partially filled with electrons but can never be empty.

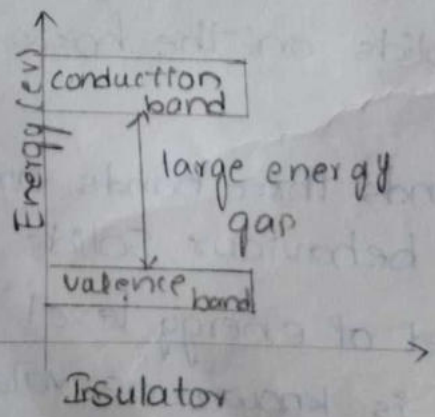
Conduction band:- A set of energy levels possesed by free electrons or conduction electrons is known as conduction band.

→ The electrons which have left the outermost orbit of an atom are called free electrons or conduction electrons.

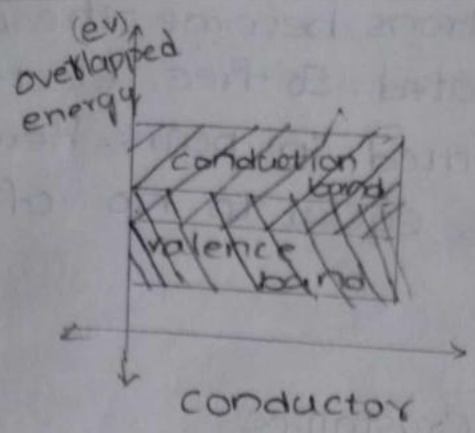
Forbidden energy band (or) energy gap:- Valence band and conduction band are Separated by a gap known as energy gap.



Eg:- Semiconductor



Insulator



Types of Semi Conductors:-

1. Intrinsic Semi conductor (Pure)
2. Extrinsic Semi Conductor (impure)

Intrinsic Semi conductor:-

→ A Semi conductor in its pure form is called an intrinsic Semi Conductor.

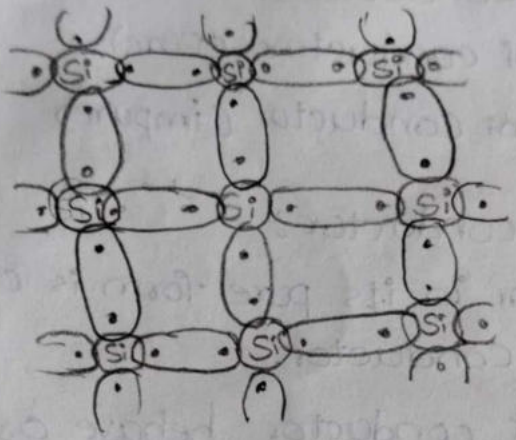
→ Intrinsic Semi conductor behave as a perfect insulator at '0' temparature

→ At room temperature some of the valence electrons absorb the thermal energy due to which they break the bond and drift to conduction band Such electrons become free to move in the crystal.

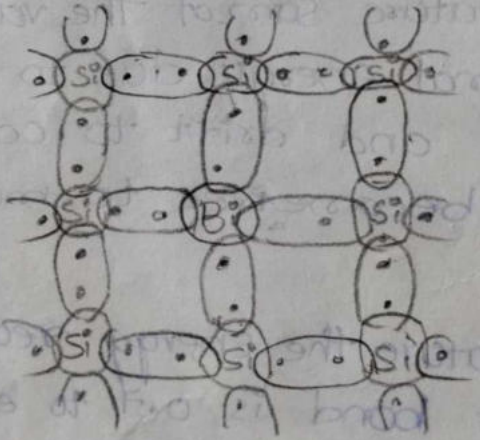
→ At room temperature the energy required to break a covalent bond is 0.7 to ev for germanium and 1.1 ev for Silicon. For every electron jumped from valence band to conduction band breaking a covalent band there will be vacancy is created in the broken band Such vacancy is called hole.

→ Whenever an electrons become the corresponding hole gets generated. So free electrons and holes gets generated in pairs. Here, the number of electrons is equal to no. of holes.

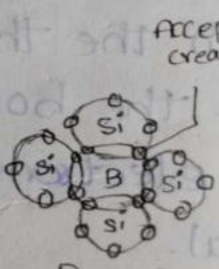
Silicon Crystalline



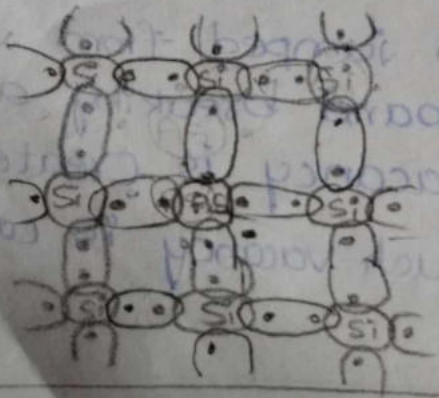
Extrinsic Semiconductor:-



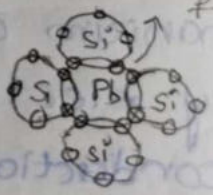
Trivalent (P type)



P-type



Pentavalent (N type)



→ The conductivity of semiconductors can be greatly improved by introducing a small no of suitable replacement atoms called impurities.

→ The process of adding impurity atoms to the pure semiconductor is called Doping. Usually, only one atom in 10^7 is replaced by a dopant atom in the doped semiconductor.

→ An extrinsic semiconductor can be further classified into:

- N-type Semiconductor
- P-type Semiconductor

Classification of Extrinsic Semiconductor.

N-Type Semiconductor

- Mainly due to electrons
- Entirely neutral
- $I = I_n$ and $n_e >> n_h$.
- Majority - Electrons and Minority - Holes.

→ When a pure Semiconductor (Silicon or Germanium) is doped by pentavalent impurity (P, As, Sb, Bi) then, four electrons out of five valence electrons bonds with the four electrons of Ge or Si.

→ The fifth electron of the dopant is set free. Thus the impurity atom donates a free electron for conduction in lattice and is called "Donor".

→ Since the no of free electron increases by the addition of an impurity, the negative charge carriers increase. Hence it is called n-type Semi conductor.

→ Crystal as a whole is neutral, but the donar atom becomes an immobile positive ion. As condoction is due to a large no of free electrons, the electrons in n-type Semi-

conductor are the Majority carriers and holes are the minority carriers.

P-Type Semiconductor

- Mainly due to holes
- Entirely neutral
- $I = I_a$ and $p_h >> p_e$
- Majority - Holes and Minority - Electrons

→ When a pure semiconductor is doped with a trivalent impurity (B, Al, In, Ga) then, the three valence electrons of the impurity bonds with three of the four valence electrons of the semiconductor.

→ This leaves an absence of electron (hole) in the impurity. These impurity atoms which are ready to accept bonded electrons are called "Acceptors".

→ With the increase in the no of impurities, holes (the positive charge carriers) are increased. Hence it is called P-type Semiconductor

→ Crystal as a whole is neutral, but the acceptors become an immobile negative ion. As conduction is due to a large no of holes, the holes in the p-type semiconductor are Majority carriers and electrons are Minority carriers.

Difference blw Intrinsic and Extrinsic Semiconductor

Intrinsic Semiconductor	Extrinsic Semiconductor
1. Pure Semiconductor	1. Impure semiconductor
2. Density of electrons is equal to the density of holes	2. Density of electrons is not equal to density of holes.
3. Electrical conductivity is low	3. Electrical conductivity is high.
4. Dependence on temparature only	4. Dependence on temp as well as on amount of impurity.

P-N Junction:

A p-n junction is an interface or a boundary blw two semiconductor material types, namely the p-type and the n-type, inside a semiconductor.

→ The p-side or the positive side of the semiconductor has an excess of holes and the n-side or the negative side has an excess of electrons.

→ In a semiconductor, the p-n junction is created by the method of doping. The process of doping is explained in further detail in the next section.

Formation of P-N Junction:

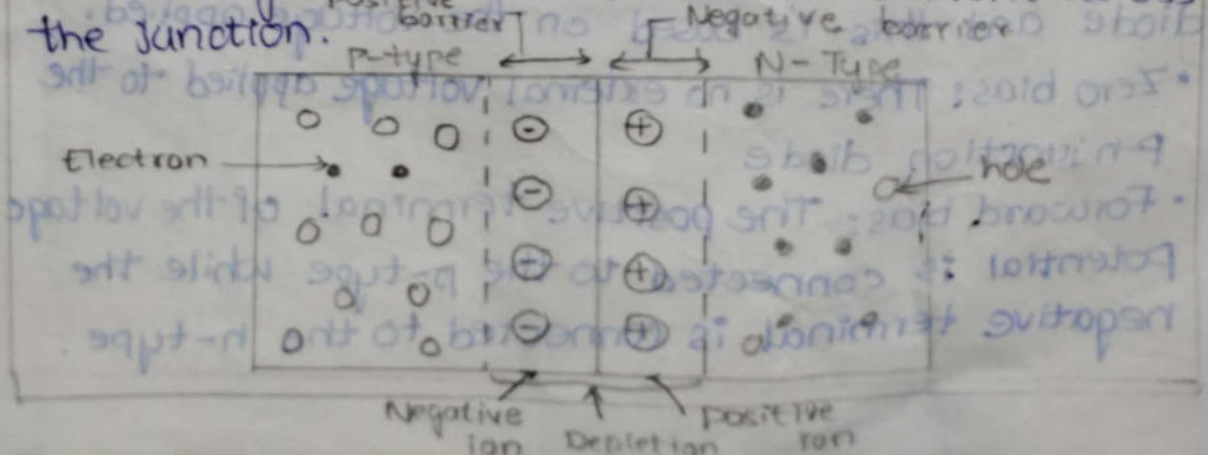
Let us consider a thin p-type silicon semiconductor sheet. If we add a small amount of pentavalent impurity to this, a part of the p-type Si will get converted to n-type silicon.

→ This sheet will now contain both p-type region & N-type region and a junction blw these two regions.

→ The processes that follow after the formation of a p-n junction are of two types - diffusion and drift.

→ As we know, there is a difference in the concentration of holes and electrons at the two sides of a junction, the holes from p-side diffuse to n-side and the electrons from the n-side diffuse to the p-side.

→ These give rise to a diffusion current across the junction.



When an electron diffuse from the n-side to the p-side, an ionized donor is left behind on the n-side, which is immobile. As the process goes on, a layer of positive charge is developed on the n-side of the junction.

→ Similarly, when a hole goes from the p-side to n-side, and ionized acceptor is left behind in the p-side, resulting in the formation of a layer of negative charges in the p-side of junction.

→ This region of positive charge and negative charge on either side of the junction is termed as depletion region.

→ Due to this positive space charge region on either side of the junction, an electric field direction from +ve charge towards -ve charge is developed.

→ Due to this electric field, an electron on the p-side of the junction moves to the n-side of junction.

→ This motion is termed as the drift, Here, we see that the direction of drift current is opposite to that of the diffusion current.

There are two operating regions in the p-n junction diode:

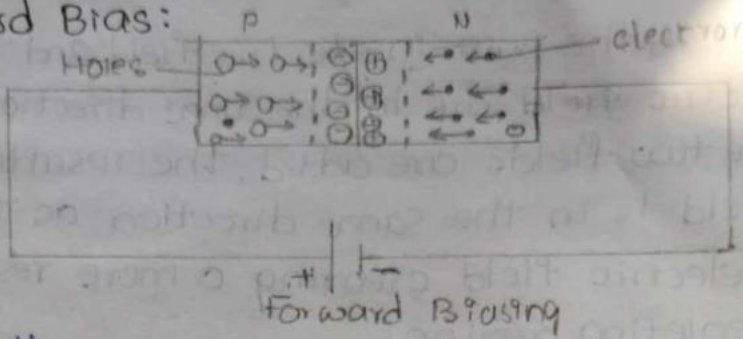
- P-type
- N-type

→ There are three biasing conditions for p-n junction diode and this is based on the voltage applied.

- Zero bias: There is no external voltage applied to the p-n junction diode
- Forward bias: The positive terminal of the voltage potential is connected to the p-type while the negative terminal is connected to the n-type.

• Reverse bias: The negative terminal of the voltage potential is connected to the p-type and the positive is connected to the n-type.

Forward Bias:



Forward Biasing

→ When the p-type is connected to the positive terminal of the battery and the n-type to the negative terminal then the p-n junction is said to be forward biased.

→ When the p-n junction is forward biased; the built-in electric field at the p-n junction and the applied electric field are in opposite directions.

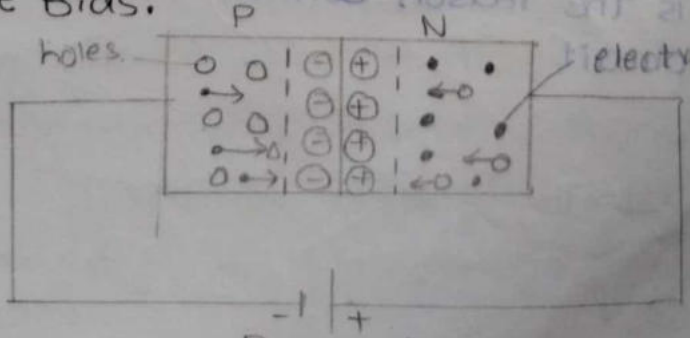
→ When both the electric fields add up the resultant electric field has a magnitude lesser than the built-in electric field.

→ This results in a less resistive and thinner depletion region.

→ The depletion region's resistance becomes negligible when the applied voltage is large.

→ In silicon, at the voltage of 0.6V, the resistance of the depletion region becomes completely negligible and the current flows across it unimpeded.

Reverse Bias:



Reverse Biasing

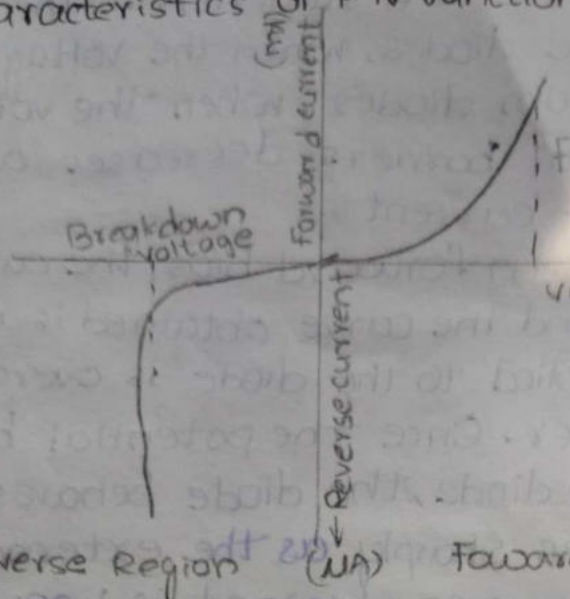
→When the p-type is connected to the negative terminal of the battery and the n-type is connected to the positive side then the P-n junction is said to be reverse biased.
→ In this case, the built-in electric field and the applied electric field are in the same direction.
→ When the two fields are added, the resultant electric field is in the same direction as the built-in electric field creating a more resistive, thicker depletion region.
→ The depletion region becomes more resistive and thicker if the applied voltage become larger

Current flow in PN junction diode

→ The flow of electrons from the n-side towards the p-side of the junction takes place when there is an increase in the voltage.
→ Similarly, the flow of holes from the p-side towards the n-side of the junction takes place along with the increase in voltage.
→ This results in the concentration gradient between both sides of the terminals.
→ Because of the formation of the concentration gradient, there will be a flow of charge carriers from higher concentration regions to lower concentration regions.
→ The movement of charge carriers inside the P-n junction is the reason behind the current flow in the circuit.

1 (a) Most IMP

I-V Characteristics of P N Junction Diode



Reverse Region Faward Region

I-V characteristics of PN Junction diode is a curve blw the voltage and current through the circuit. Voltage is taken along the x-axis while the current is taken along the y-axis. The above graph is the I-V characteristics curve of the PN Junction diode. With the help of the curve we can understand that there are three regions in which the diode works, and they are:

- Zero bias
- Forward bias
- Reverse bias.

→ When the PN junction diode is under Zero bias condition, there is no external voltage applied and this means that the potential barrier at the junction does not allow the flow of current.

→ When the PN junction diode is under forward bias condition, the P-type is connected to the positive terminal while the n-type is connected to the negative terminal of the external voltage.

→ In this manner, there is a reduction in the potential barrier. For Silicone diodes, when the voltage is 0.7 V and for germanium diodes, when the voltage is 0.3V, the potential barriers decreases and there is a flow of current.

→ When the diode is in forward bias, the current increases slowly and the curve obtained is non-linear as the voltage applied to the diode is overcoming the potential barrier. Once the potential barrier is overcome by the diode, the diode behaves normal and the curve rises sharply as the external voltage increases & the curve so obtained is linear.

→ When the PN junction diode is under reverse bias condition, the P-type is connected to the negative terminal while the n-type is connected to positive terminal of the external voltage. This results in an increase in the potential barrier. Reverse saturation current flows in the begining as minority carriers are present in the junction.

→ When the applied voltage is increased, the minority charges will have increased kinetic energy which affects the majority charges. This is the stage when the diode breaks down. This may also destroy the diode.

Applications of PN Junction Diode

- P-n junction diode can be used as a photodiode as the diode is sensitive to the light when the configuration of the diode is reverse-biased.
- It can be used as a solar cell.
- When the diode is forward-biased, it can used in LED lighting applications.
- It is used as rectifiers in many electric circuits and as a voltage-controlled oscillator in varactors.

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Diode Resistance:-

Diode conducts current in forward biased mode whereas as reverse biased diode doesnot conduct current so that diode offers low resistance in forward biased when compared to reverse biased resistance. The resistance offered by a diode under forward bias is known as Forward Resistance. It is of two types.

1. DC or static Resistance
2. AC or Dynamic Resistance

DC or Static Resistance:-

The resistance offered by a diode under dc conditions is called DC Resistance.

$$R_{static} = \frac{V}{I}$$

The static resistance under the forward bias is denoted by R_f while under reverse bias is denoted by R_r.

$$R_f = \frac{V_f}{I_f}$$

$$R_r = \frac{V_r}{I_r} \Omega = \frac{V_r}{I_0} \Omega$$

Ac or Dynamic Resistance:-

The resistance offered by a diode under AC conditions is called AC Resistance.

(or)

It is defined as the ratio of change in forward voltage to change in forward current.

$$r_d = \frac{dV}{dI}$$

From diode current equation $I = I_0(e^{V/\eta V_T} - 1)$

Where I_0 = Inverse Saturation current

V = Applied voltage

$V_T = \frac{kT}{q}$ = Voltage equivalent of temparature in volts.

T = Absolute temperate

K = Boltzamns constant = 8.62×10^{-5} ev/°k

η = constant for germanium (ge = 1) & (Si = 2).

$$I = I_0 \cdot e^{V/\eta V_T} - I_0 \rightarrow (1)$$

$$I + I_0 = I_0 \cdot e^{V/\eta V_T} \rightarrow (2)$$

diff eqn (1) w.r.t to V

$$\frac{dI}{dV} = \frac{d}{dV}\left(I_0 \cdot e^{V/\eta V_T} - I_0\right)$$

$$\frac{dI}{dV} = I_0 \cdot e^{V/\eta V_T} \cdot \frac{1}{\eta V_T} - 0$$

$$\frac{dI}{dV} = \frac{I_0}{\eta V_T} e^{V/\eta V_T}$$

$$\frac{dI}{dV} = \frac{I + I_0}{\eta V_T} \quad (I_0 << I)$$

$$\therefore \frac{dI}{dV} = \frac{I}{\eta V_T}$$

$$r_d = \frac{dV}{dI} = \frac{\eta V_T}{I}$$

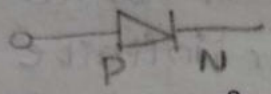
$$\boxed{r_d = \frac{\eta V_T}{I}}$$

MID-1 2nd P

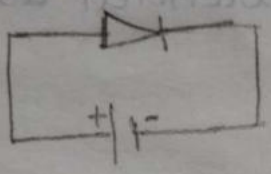
Diode Equivalent Circuit:

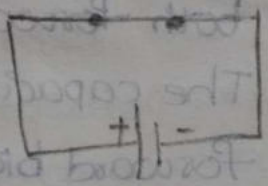
An ideal diode offers zero resistance in the forward biased condition whereas it offers infinite resistance in the reversed biased condition. So that ideal diode is replaced by a conductor in forward bias. While in the reverse bias it is replaced by an open circuit.

Symbol:

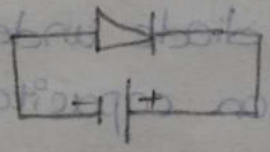


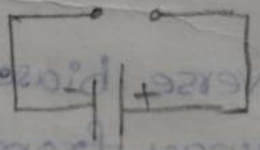
Ideal diode under forward bias



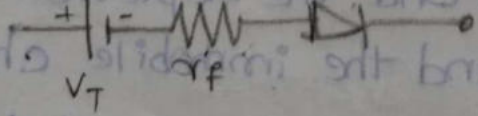


Ideal diode under reverse bias

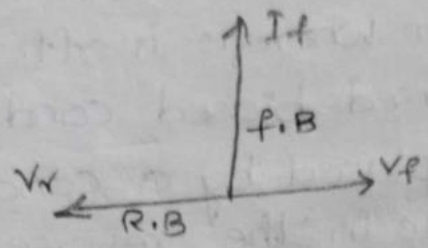




Equivalent circuit [Practical Diode equivalent circuit]



Ideal diode characteristics



Practical diode has Small resistance in forward bias, While under reverse bias it has maximum resistance. But not under infinite so that a practical diode is represented with series resistance and barrier potential as Source "V_T".

Diode Capacitance:

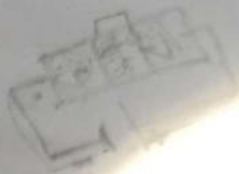
Diode offers capacitance in both forward bias as well as in reverse bias. The capacitance offered by a diode under forward bias is known as Diffusion capacitance. And the capacitance offered by a diode under reverse bias is known as Transition capacitance

Transition capacitance:-

When a P-N junction is reverse biased the majority carriers move away from the junction. As result the depletion region width will be increased. Ond the depletion region acts as insulator and the immobile charges will (like) be increases on either side of depletion region. This uncovered incremental charge can be considered as transition capacitance and is given $C_T = \frac{dQ}{dV}$

*It occurs due to majority carriers.

$$C_T = \frac{dQ}{dV} \qquad C_T = \frac{\varepsilon A}{W}$$



Where C_T = Transition capacitance

$\frac{dQ}{dV}$ = Increase in charge due to increase in voltage.

If we increase reverse bias the transition capacitance will be decreases as they increases in reverse bias increase depletion region width.

Diffusion Capacitance:

When a P-N junction is forward bias the electrons from N side enter the P-side and holes from P side enter into the N-side and gets recombine The density of charge carriers is high near the junction and decays exponetially with distance thus a charge is stored on both sides of the junction. This charge we are considering as diffusion capacitance or storage capacitance

$$C_d = \frac{dQ}{dV}$$

$$I = Q/\tau$$

$$Q = I\tau$$

Where τ is the lifetime of charge

I = diode current.

$$Q = I\tau$$

$$Q = I_0 e^{V/\eta V_T} \cdot \tau$$

$$C = \frac{dQ}{dV}$$

$$= \frac{d}{dv}\left(I_0 \cdot e^{v/\eta V_T} \cdot \tau\right)$$

$$= I_0 \tau \cdot \frac{1}{\eta V_T} \cdot e^{v/\eta V_T}$$

$$C = \frac{I_0 \tau}{\eta V_T} e^{v/\eta V_T}$$

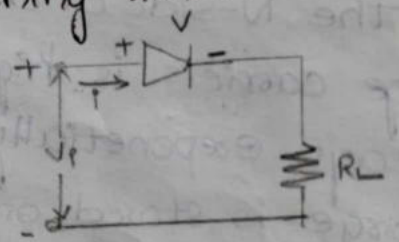
$$C = \frac{\tau}{\eta V_T} \cdot I_0 \cdot e^{v/\eta V_T}$$

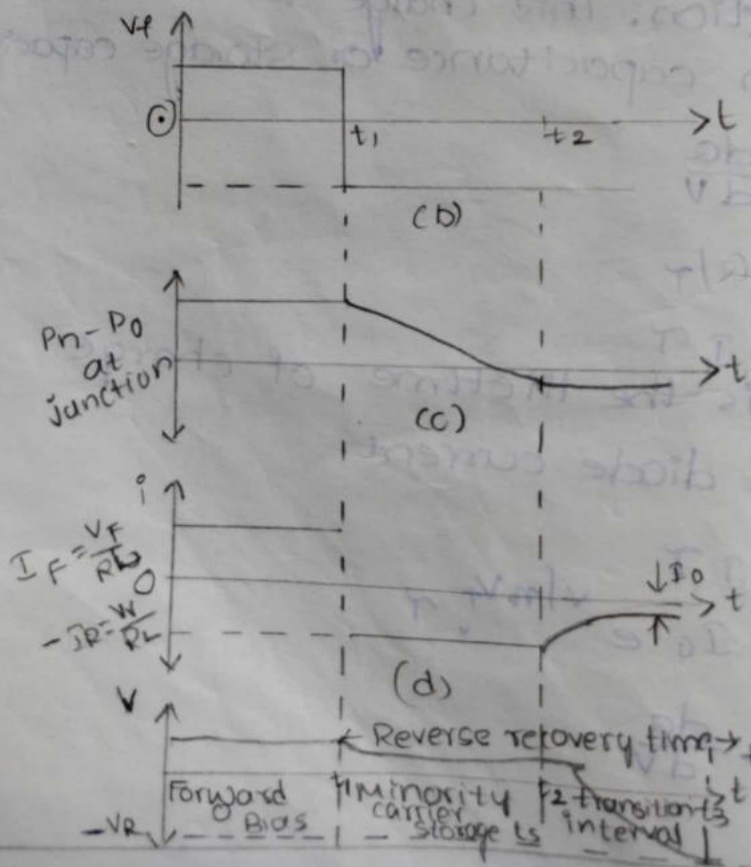
$$= \frac{\tau (I + I_0)}{\eta V_T}$$

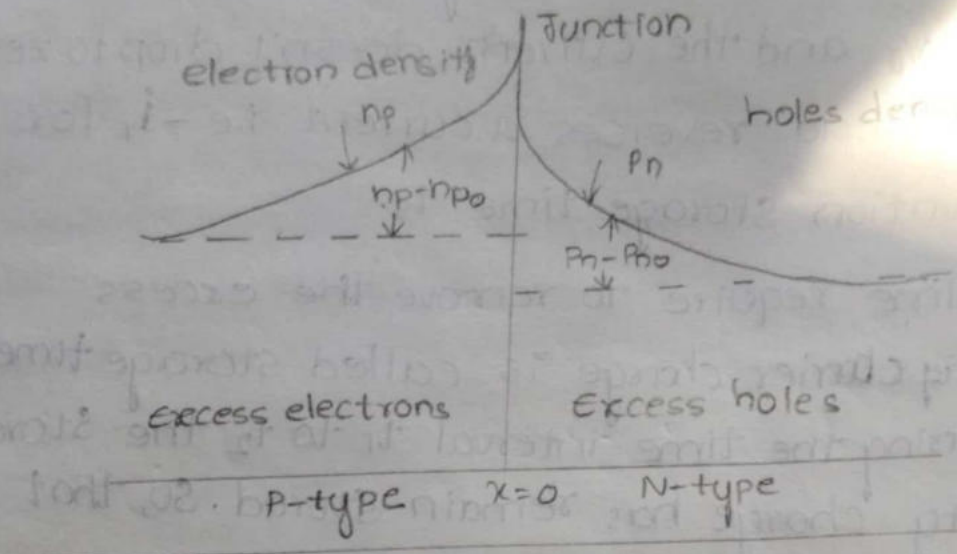
$I_0 << I$

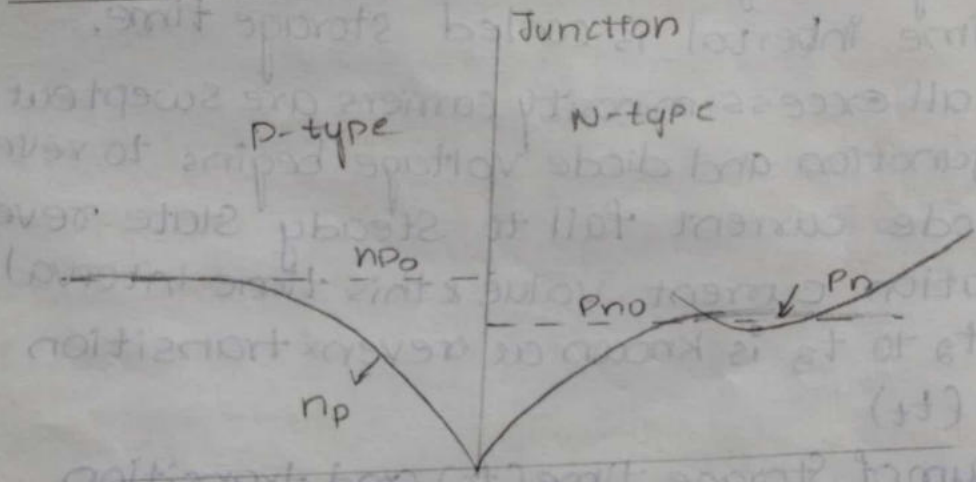
$$C_D = \frac{\tau I}{\eta V_T}$$

Diode Switching Times :-









Diode as a Switch

A Diode is two terminal P-N junction. The P-N Junction when forward biased acts as closed circuited and when reversed biased acts as open circuited. Hence, change in state from forward biased to reverse biased makes the diode work as a switch the forward being on & reverse being off.

Switching times:-

→Upto time t_1 the diode is conducting in forward direction and current flows through the diode and there is a voltage drop across the diode.

→ At time t_1, the input voltage reverses to a value $-V_R$ and the current doesn't drop to zero but instead reverses a current i.e $-I_r$ for the duration storage time t_s.

→ The time require to remove the excess minority carrier charge is called storage time (t_s) or during the time interval t_1 to t_2 the stored minority charge has remain stored. So, that this time interval is called storage time.

→ After all excess minority carriers are swept out of the junction and diode voltage begins to revers and diode current fall to steady state reverse saturation current value & this time interval from t_2 to t_3 is known as reverse transition time (t_t)

→ The sum of storage time (t_s) and transition time (t_t) is called the diode reverse recovery time (t_{rr}).

$$t_s + t_t = t_{rr}$$

→ The time required for the diode to change from forward bias to reverse bias is called as reverse recovery time.

→ The time required for the diode to change from reverse bias to forward bias is called as forward recovery time.

1. In a silicon diode the forward current changes by 2.5 mA when the voltage changes from 0.08 to 0.09 V then find the dynamic resistance of diode.

Given $\Delta V = 0.09 - 0.08\ V$

$\Delta I = 2.5\ mA$

$$r_d = \frac{\Delta V}{\Delta I} = \frac{0.01}{2.5 \times 10^{-3}} = \frac{0.01}{2.5} \times 10^{3}$$

$$= 0.004 \times 10^{3}$$

$$= 4\ \Omega$$

2. The P-N Junction diode voltage is changing from 5V to 15V then the value of current changes from 38 μA to 88 μA. Determine the resistance of junction diode.

Given $\Delta V = 15 - 5 = 10\ V$

$\Delta I = 88\mu A - 38\mu A = 50\mu A$

$$r_d = \frac{\Delta V}{\Delta I} = \frac{10}{50 \times 10^{-6}}$$

$$= \frac{10 \times 10^{6}}{50}$$

$$\frac{10^{7}}{5 \times 10^{1}}$$

$$= \frac{10^{6}}{5}$$

$$= 200000$$

$$= 200 \times 10^{3}$$

$$r_d = 200\ K\Omega$$

3. An ideal germanium diode at room temperature as source resistance of 4.57Ω at a point where the current flowing is 43.8mA. Find the dynamic resistance for a forward bias 0.1volts

Given $r_s = \frac{V}{I}$

$$4.57 = \frac{V}{43.8\times10^{-3}}$$

$$V = 0.2V$$

$$\Delta V = V_2 - V_1 = 0.0 - 0.1 = 0.1V$$

$$r_d = \frac{\Delta V}{\Delta I} = \frac{0.1}{43.8\times10^{-3}} = \frac{500}{219}$$

$$= 2.28\Omega$$

4. Determine the static and Dynamic resistance of a P-N junction germanium diode for an applied forward bias 0.2V if the temperature is 300k under reverse saturation current is 1μA.

Given that,

$V = 0.2V$ $\quad \eta = 1$ for germanium

$I_0 = 1\times10^{-6}A$ $\quad V_T = \frac{KT}{q} = \frac{8.62\times300\times10^{-5}}{1.6\times10^{-19}}$

$I = I_0 \cdot e^{V/\eta V_T} - I_0$ $\quad = 26mV$

$$I = 1\times10^{-6} e^{\frac{0.2}{26\times10^{-3}}} - 1\times10^{-6}$$

$$= 1\times10^{-6}\left(e^{0.2/26\times10^{-3}} - 1\right)$$

$$= 1\times10^{-6}\left[e^{100/13} - 1\right) = 1\times10^{-6}(e^{7.69} - 1)$$

$= 1 \times 10^{-6} (2186.3 \rightarrow 0)$

$= 2.18 \times 10^{-3} A$

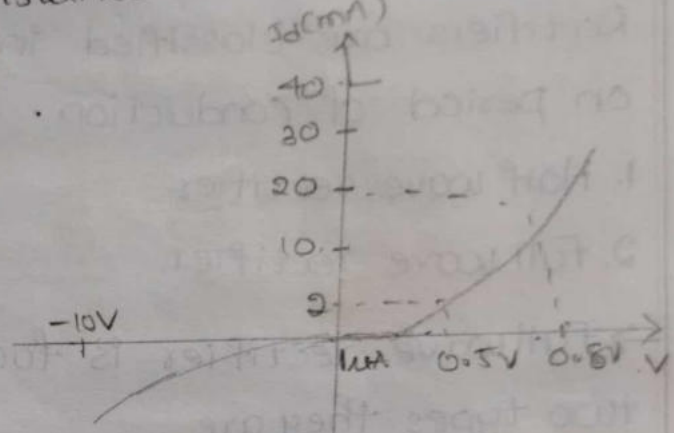
$= 2.18 mA$

$r_{static} = \frac{V}{I} = \frac{0.2}{2.18 \times 10^{-3}} = 91.74 \Omega$

$r_d = \frac{\Delta V}{\Delta I} = \frac{\eta V_T}{I} = \frac{26 \times 10^{-3} \times 1}{2.18 \times 10^{-3}} = 11.9 \Omega$

5. Determine the DC resistance levels for the diode at

1. $I_d = 2mA$
2. $I_d = 20mA$
3. $V_d = -10V$



1. $I_d = 2mA$

$V_d = 0.5V$

$r_d = \frac{V}{I} = \frac{0.5}{2 \times 10^{-3}} = 250 \Omega$

2. $I_d = 20mA \quad V_d = 0.8V$

$r_d = \frac{V}{I} = \frac{0.8}{20 \times 10^{-3}} = 40 \Omega$

3. $V_d = -10V \quad I_d = 1 \times 10^{-6}$

$r_d = \frac{V_d}{I_d} = \frac{-10}{1 \times 10^{-6}} = -10000000$

$= -1 \times 10^{7}$

$= -10 \times 10^{6}$

$= -10$ megha ohms