UNIT-1 Syllabus:

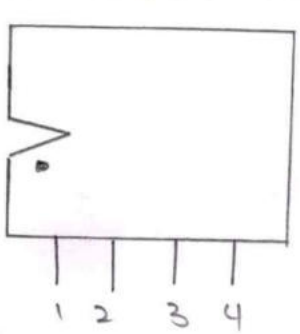
Integrated circuits and operational Amplifier: Introduction, classification of Ic's, IC chip size and circuit complexity, Basic Information of op-amp IC 741 and its features, the ideal operational amplifier, Op-amp internal circuit, Op-Amp characteristics - DC and AC, features of 741 Op-amp.

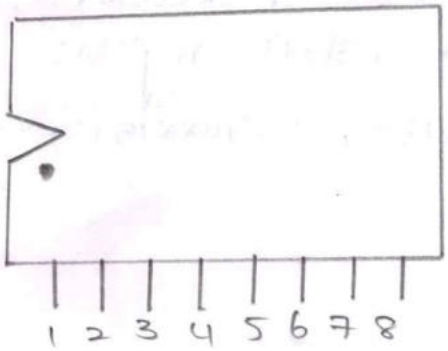
Introduction:

Integrated circuit:

Integrated circuit is a miniature, low cost electronic circuit consisting of both active and passive elements are fabricated on a single silicon chip.

* Integrated circuits (Ic) plays a very important role in Electronics.
* Most of the Ic's Specially made for a specific task and contains upto thousands of Transistors, Diodes & Resistors.
* Special purpose Ic's such as Audio Amplifiers, FM radios, logic blocks, regulators and even a whole micro computer in the form of a micro controller can be fitted inside a tiny package
* Some of simple integrated circuits are shown in below figure.





Advantages of Ic:

* Low cost
* High speed
* Compact in size
* Low power consumption
* Increased realibility

Disadvantages of Ic:

* Ic's are irrepairable
* fault identification is difficult

* Classification of Integrated circuit:

1. According to the operation:

1. Analog Ic's
2. Digital Ic's

Analog Ic's (Linear Ic's):

These Ic's takes continuous time period signals as input and process them to provide continuous time period signals as the output

Ex: Amplifiers, Oscillators, filters, multivibrators, Integrator, Differentiator etc..

Ic 741, Ic 555 etc

Digital Ic's (Non-linear Ic's):

The Integrated circuit which takes digital signals as the input and process them to provide digital Outputs is known as digital Ic's.

Ex: multiplexers, decoders, encoders, counters, comparators, shift registors etc.

Ic 74xx138, Ic 74xx151 etc.

II. classification according to the complexity of the circuit

Type of Ic	Generation	year of Invention	NO of transistors	Applications :
SSI	1st	1964	1 to 100	Logic gates
MSI	2nd	1968	10 to 500	multiplexers, decoders etc
LSI	3rd	1971	500 to 20000	RAM, ROM etc
VLSI	4th	1980	20000 to 1 lakh	digital cameras, Tabs, Pc, Graphic card etc
ULSI	5th	1984	>1 lakh	Special purpose Registers, General purpose Registers, etc.

III According to the manifacturing

1. monolithic
2. Hybrid

IV. Types of packages

1. Flat type
2. Metal can
3. DIP package
4. Quad type

V. According to the Applications

1. General purpose Ic's
2. Special purpose Ic's

* **Basic Information of OP-Amp:**

An Operational Amplifier is a direct coupled high gain amplifier usually followed by a level translater and an output stage

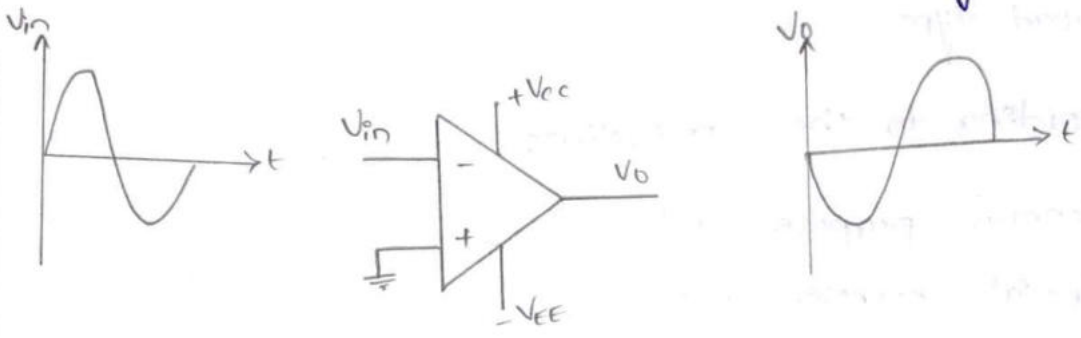
* The op-amp is a versatile device that can be used to amplify both AC & DC signals and that was generally designed for performing different mathematical operations such as addition, subtraction, Integration, Differentiation etc.

* Op-amp has 2 input of opposite polarities and it has single output and has 2 power supplies

* Almost all the op-amp have atleast 5 terminals
  a. The positive supply voltage terminal $+V_{cc}$
  b. Negative supply voltage terminal $-V_{EE}$
  c. Output terminal
  d. Inverting Input terminal (-)
  e. Non-Inverting input terminal (+)

* The input at inverting terminal is positive voltages the output is -ve voltage and vice versa

* While the input at non-inverting terminal results is the same polarity output signal at the output terminal. This is shown in below fig



Input is applied to the Inverting terminal

1. Input Stage:

The input stage requires high i/p impedance to avoid loading on the sources. It requires 2 i/p terminals & also it requires low o/p impedance

* Such all requirements are achieved by using dual i/p balanced o/p differential amplifier at the i/p stage.
* This stage provides most of the voltage gain of the amplifier & also establishes the i/p resistance of the amplifier

2. Intermediate stage:

The o/p of the i/p stage drives the next stage which is an intermediate stage. this is another differential amplifier with dual i/p unbalanced o/p ie., single ended o/p

* the overall gain requirement of the op-amp is very high
* In most of the amplifier an Intermediate stage is a dual i/p unbalanced o/p differential amplifier. This stage increases voltage gain of the amplifier

3. Level shifting stage.

The Level shifting stage is used after the interme-diate stage to shift the dclevel at the o/p of the intermediate stage downward to zero volts w.r.t ground

* Here coupling capacitors are not used to couple the amplifiers in the intermediate state. Dc biasing voltage level propagates through the amplifier. Due to this a Significant dc level appears at the o/p along with ac o/p
* Due to this effect o/p gets distorted & limits the maximum o/p voltage. this is shown in below fig

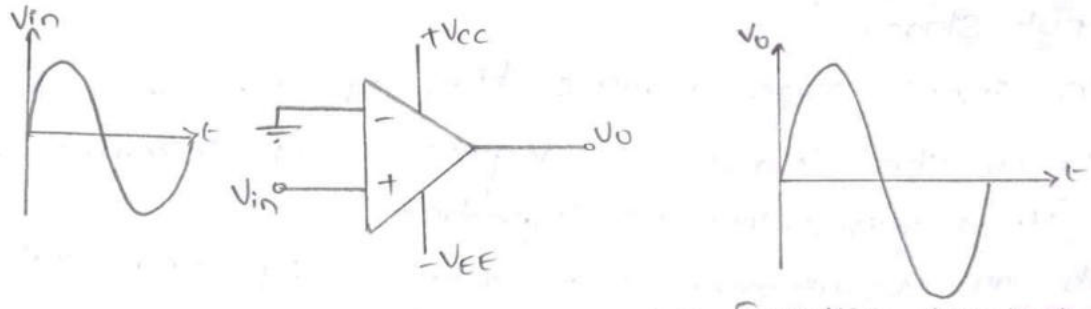
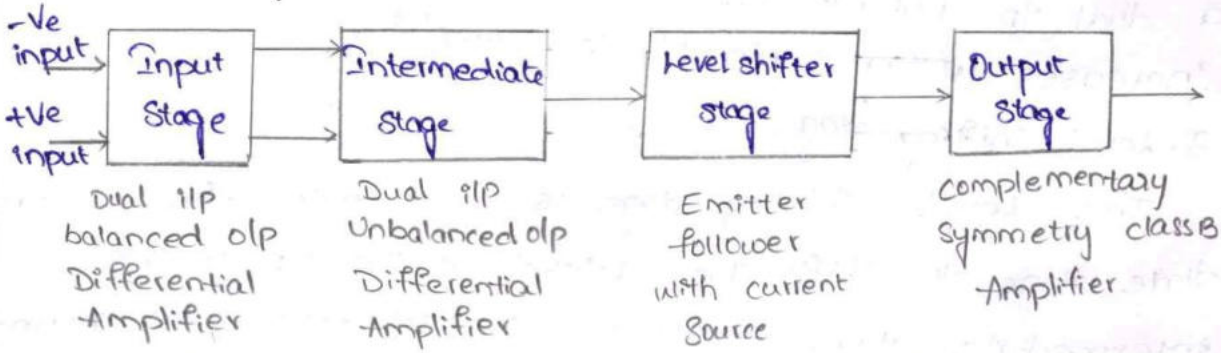


fig: Input is applied to the Non-Inverting terminal

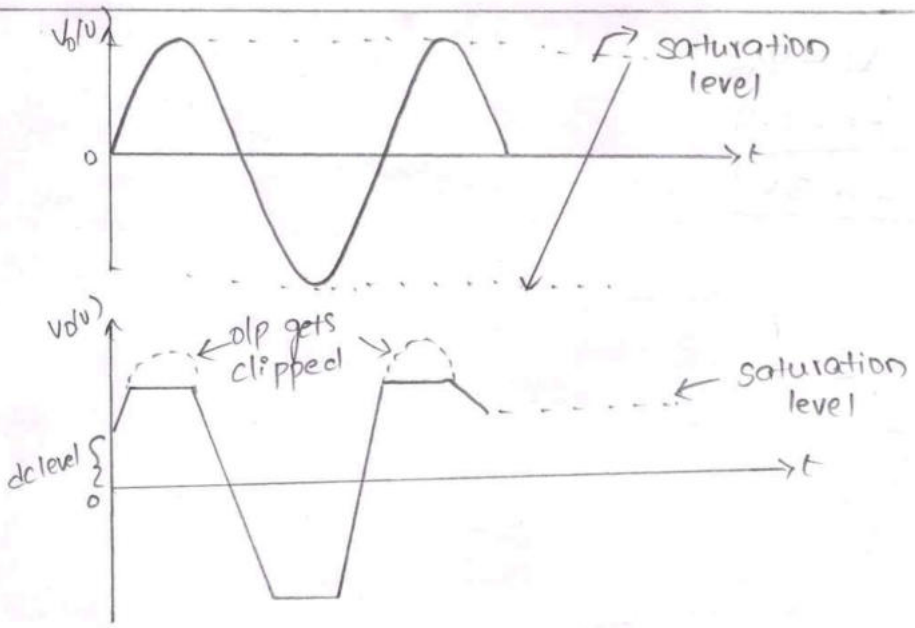
* The op-amp works on dual power supply
* The dual power supply is generally balanced ie., the voltage of the +ve supply $+V_{cc}$ and -ve supply $-V_{EE}$ are in same magnitude. The typically used power supply voltages are $\pm 15V$.
* But if the 2 voltage magnitudes are not equal in a dual supply it is called as unbalanced power supply
* But almost we use the balanced dual power supply for op-amp in practically

Block Diagram of OP-Amp:



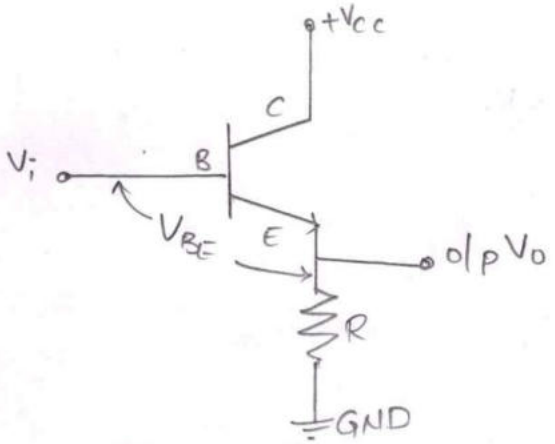
The fig. shows the block diagram of op-amp. It consists of 4 cascaded blocks.

1. Input stage
2. Intermediate stage
3. Level shifter
4. Output stage



* So the main purpose of the level shifting stage is to shift the o/p 'Q' point dc level towards the ground with minimum change in the ac signal.
* this also satisfies that the o/p should have equal voltage level of 0V for '0' i/p signal.

Eg: 1. How to vary o/p by giving i/p



Applying KVL to the i/p side

$$V_i - V_{GS} - V_o = 0$$

$$\boxed{V_o = V_i - V_{GS}}$$

By varying i/p, the o/p is decreasing

Proof: Let us assume that

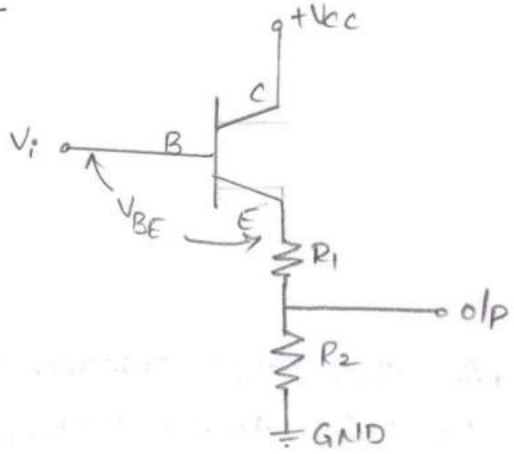
$$V_i = 5V, \quad V_{GS} = V_{BE} = 0.7V$$

$$V_o = V_i - V_{GS}$$

$$= 5 - 0.7$$

$$\boxed{V_o = 4.3\,V}$$

Eg : 2



Applying KVL to the circuit

$$V_i - V_{BE} - I(R_1 + R_2) = 0$$

$$I(R_1 + R_2) = V_i - V_{BE}$$

$$I = \frac{V_i - V_{BE}}{R_1 + R_2}$$

$$\frac{V_o}{R_2} = \frac{V_i - V_{BE}}{R_1 + R_2} \times R_2$$

Proof: Let us assume

$$V_o = \frac{5 - 0.7}{10 + 4} \times 4$$

$$= \frac{4.3 \times 4}{14}$$

$$V_o = \frac{17.2}{14}$$

$$V_o = 1.22 \quad V_o \downarrow$$

4. Output stage:

The last stage is a complementary class B pushpull amplifier. The basic requirements of an o/p stage are low o/p impedence.

1. Large o/p voltage
2. Large o/p current
3. Low o/p impedance
4. Low power dissipation
5. Short circuit protection.

A pushpull amplifier satisfies the above requirements & hence commonly used in the o/p stage of an Op-amp.

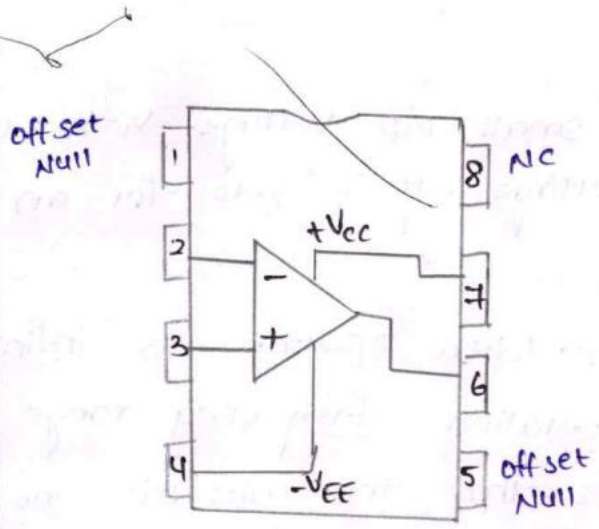
* Packages and Pinouts:

The Op-amp is fabricated on a very small silicon chip and is package in a suitable case.

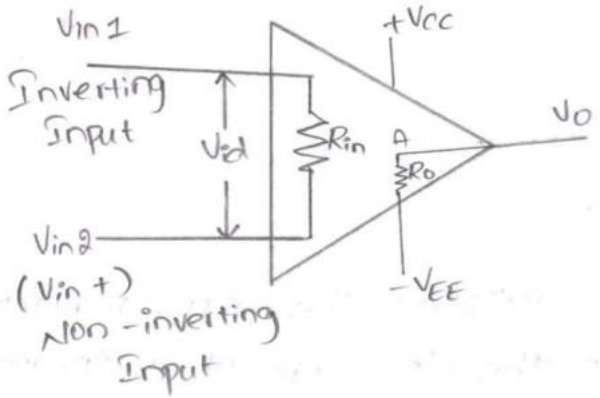
The Op-amp is generally available in 2 packages

1. Metal can
2. DIP (Dual in line package)

→ Metal can's are available with 8, 10 or 12 pins
→ DIP packages are having 8 (or) 14 Pins.
→ DIP package is most widely used.



Equivalent circuit of op-amp:



$V_o = A(V_{id})$

$V_o = -A(V_{in1} - V_{in2})$

* Characteristics of an Ideal Op-Amp:

1. Infinite input Resistance:

It is denoted by R_i and it is infinite for an Ideal op-amp. this ensures that no current can flow into an ideal op-amp

2. Infinite voltage Gain:

It is denoted by A_{OL} (or) A. It is infinite for an ideal op-amp

3. Zero o/p Impedance:

It is denoted by R_o. It is Infinite for an Ideal op-amp

4. Zero offset voltage:

The presence of the small o/p voltage $V_1 - V_2 = 0$ is called as an offset voltage. It is zero for an ideal op-amp.

5. Infinite Band Width:

The Band Width of an Ideal op-amp is infinite. This means that the operating frequency range is from 0 to ∞. This ensures that the gain of the op-amp remains constant over the frequency range from dc to infinite frequency. Therefore an op-amp can amplify dc as well as ac signals

6. Infinite CMRR:

It is defined as the ratio of differential gain and common mode gain. It is infinite for an ideal op-amp.

$$CMRR = \frac{A_D}{A_C}$$

7. Slew Rate:

It is defined as the maximum rate of change of o/p voltage w.r.t time. It is Infinite for an Ideal op-amp It is denoted by 's'

$$S = \frac{dV_0}{dt}$$

Pratical op-Amp:

The characteristics of an Ideal op-amp can be approximated closely enough, for many pratical op-amp characteristics are little but different than the ideal op-amp characteristics.

1. Input Resistance:

It is denoted by R_i. It has large value in practical op-amp. The typical value of op-amp is $2M\Omega$

2. Open loop Gain:

It is the voltage gain of an op-amp when no feedback is applied, pratically it is large

3. Output Impedence:

It is denoted by R_0. It has very small value. The typical value of o/p resistance is few ohms i.e., 1Ω or 2Ω etc

4. Bandwidth

The Bandwidth of a pratical op-amp is very small but if we apply -ve feedback it can be increased to a desired value.

* DC characteristics :

We have four different DC characteristics. They are

1. Input Bias current
2. Input offset current
3. Input offset voltage
4. Input & Thermal Drift

1. Input Bias current :

The average value of 2 currents flowing into the Op-amp input terminals is called input bias currents. It is denoted by I_B. this is shown in below fig

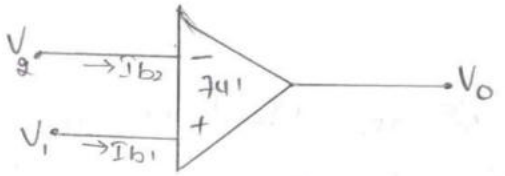


fig: Input Bias currents

Mathematically, it is expressed as

$$I_B = \frac{I_{b1} + I_{b2}}{2}$$

→ Ideally it should be zero, pratically it should be $I_B = 200nA$

2. Input offset current :

It is defined as the algebric difference between the currents flowing into the 2 i/p terminals of the op-amp. It is denoted by I_{ios}.

Mathematically it is given by

$$I_{ioc.} = I_{b1} - I_{b2}$$

3. Input offset voltage :

The differential voltage must be applied blw the 2 i/p terminals of an op-amp, to make the o/p voltage zero is called as input offset voltage. It is denoted by V_{ios}

→ Whenever both the i/p terminals of the op-amp are grounded ideally the o/p voltage should be zero. However, in this condition the pratical op-amp shaos be zero. a small non-zero o/p voltage. This is due to mis-matching present in the internal circuit of an op-amp. Such a voltage can cause error in the practical applications, for which op-amp is used

→ To make such a voltage to zero, it is necessary to apply small difference voltage blw the 2 i/p terminals of an op-amp.

This voltage is called i/p offset voltage

4. Thermal Drift:

Bias current offset current (I_{IOS}), offset voltage (V_{IOS}) change with temperature. A circuit designed at 25°C may not remain so when temperature raises to 35°C. This is called drift

→ Op-amp offset current drift is expressed nA/°c and offset voltage drift is expressed in mV/°c

→ There are very few circuit techniques that can be used to minimize the effect of drift

1. printed circuit board layout (PCB)
2. Forced air cooling

1. PCB Layout:

It can be used to keep op-amp away from source of heat

2. Forced air cooling

It may be used to stabilize the temperature

Ac characteristics:

CMMR

1. Common mode Gain:

When the same input voltage is applied to both input terminals of an op-amp, then the op-amp said to be operate in common mode configuration.

$\therefore$ common mode gain $= \frac{V_{ocm}}{V_{cm}} = A_{cm}$

Differential voltage Gain:

When ever two different inputs given to the op-amp then the op-amp is said to be operating in differential mode configuration

$$\therefore A_D = \frac{V_o}{V_{id}}$$

* The CMMR is defined as the ratio of differential gain to the common mode gain

$$\therefore CMRR = \frac{A_D}{A_{CM}}$$

2. PSRR or SVRR supply voltage Rejection Ratio

It is defined as the change in an op-amp input offset voltage V_{io} caused by the variations in supply voltage is known as supply voltage Rejection Ratio

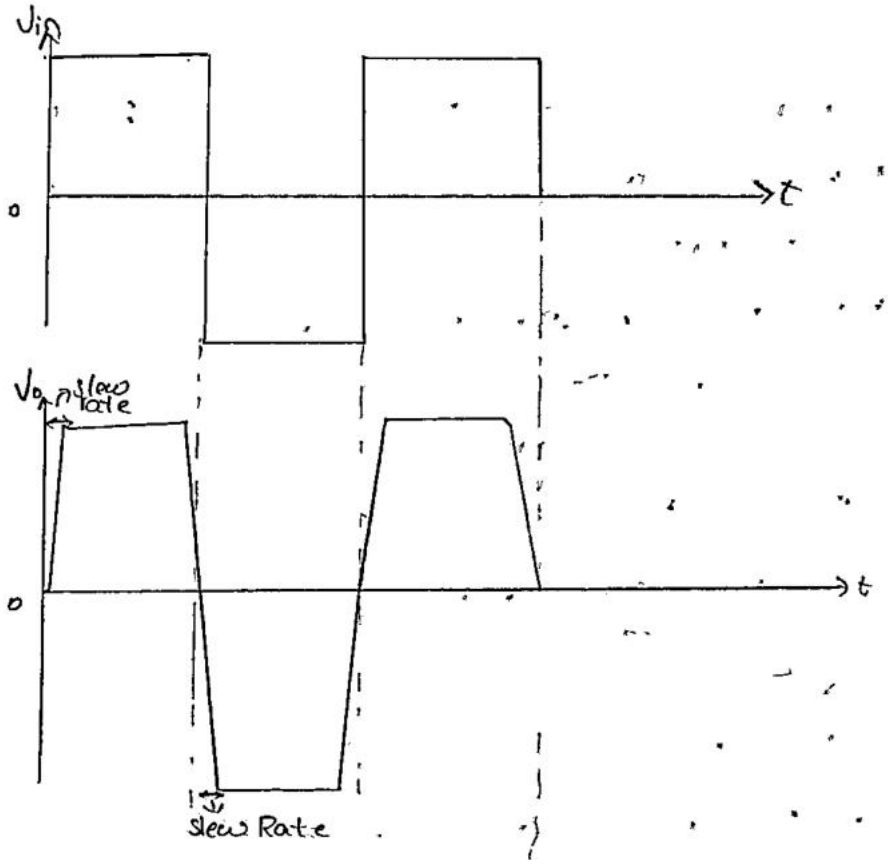
$$SVRR = \frac{\Delta V_{IO}}{\Delta \text{power supply}}$$

3. Slew Rate:

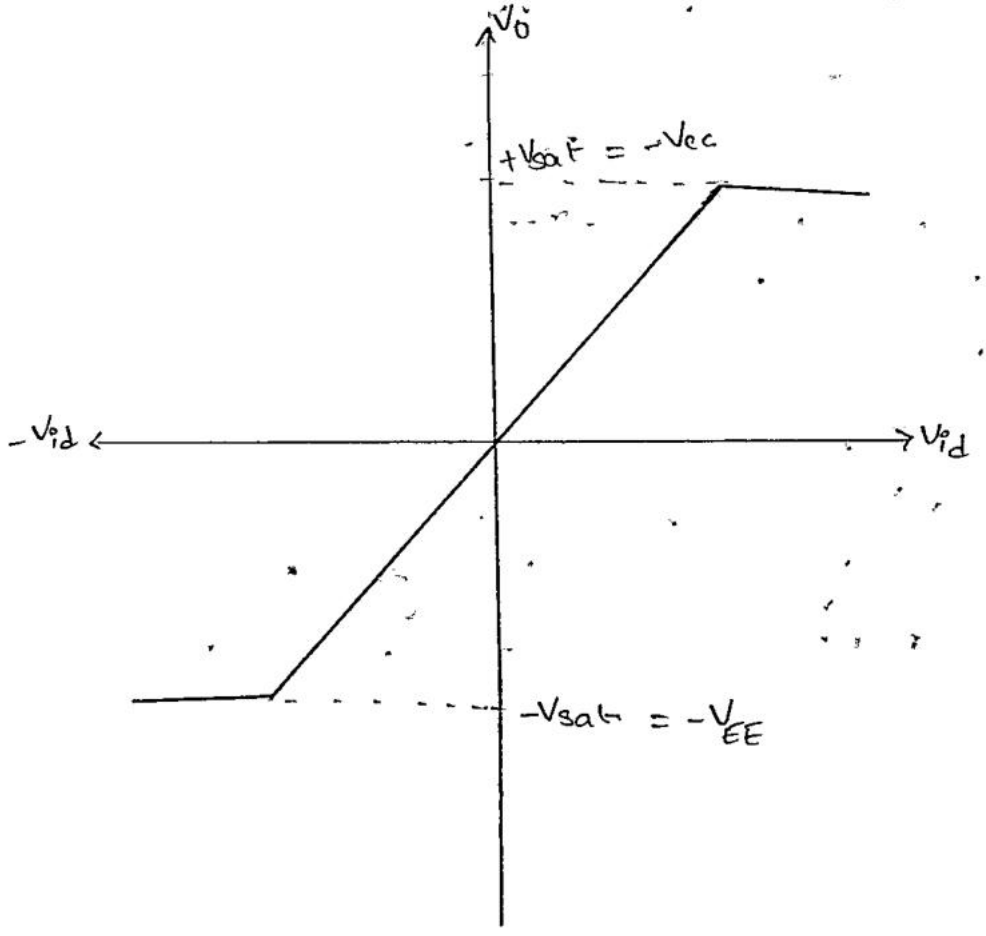
It is defined as the maximum rate of change of output voltage per unit time is known as slew rate

* It is expressed in terms of volts / micro second

$$\text{Slew Rate} = \frac{dV_o}{dt} \quad \text{volts/microsecond}$$



* Transfer characteristics of Ideal op-Amp.



* **Features of 741 op-Amp:**

The following are the features of 741 op-Amp

1. No latchup problem
2. Short circuit protection
3. No frequency compensation circuits Required
4. Low power consumption
5. Large common mode gain
6. Offset Null capability

* **Specifications of 741 Ic op-Amp:**

* Applications:
  1. Military Application → -50°c to +125°c
  2. Industrial Application → 0°c to 75°c & -25°c to +80°c
  3. Commercial Application → 0°c to 50°c & 0°c to 75°c
* Input offset voltage = 6 mv
* Input offset current = 200 nA
* Input Bias current = 500nA
* Input Resistance is 2 MΩ
* Output Resistance 75Ω
* CMMR 90dB
* SVRR 150 μv/v
* slew rate 0.5 v/μsec
* offset voltage adjustment range ±15mv
* power consumption of 741 Ic is 85 mwatts.

UNIT - II

Applications of OP-AMPs.

Linear Applications of Op-Amp :

Inverting Amplifier :

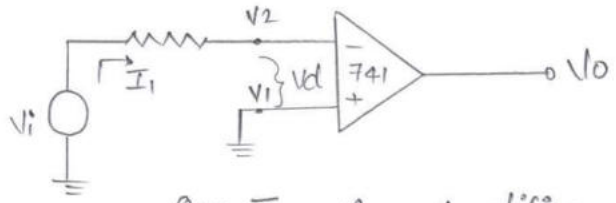


fig: Inverting Amplifier

→ In this the input is applied at inverting terminal and the Non-inverting terminal is grounded.

→ In this the output is out of phase (180° phase shift) with the input.

→ We know that, Open loop gain,

$$A = \frac{V_o}{V_d}$$

Where, $V_d = V_1 - V_2$

So, $A = \frac{V_o}{V_1 - V_2}$

$$V_o = A(V_1 - V_2)$$

If source resistance Ri is very small, then it is neglected

$\therefore V_2 = V_1$

$$V_o = A(V_1 - V_i)$$

from fig, $V_1 = 0$ ($\because$ it is connected to ground)

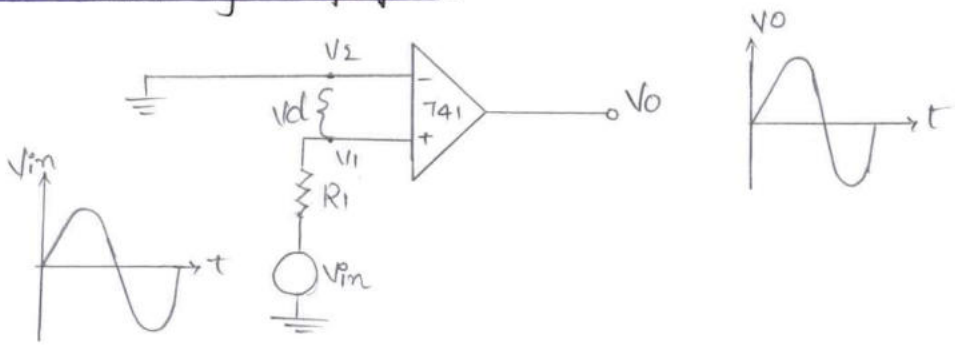
$$V_o = A(0 - V_i)$$

$$\therefore V_o = -AV_i$$

Where, -ve sign indicates that phase shift provided in between input and output.

The above equation says that the o/p voltage 'A' times larger (or) increased then the input.

Non - inverting Amplifier:



→ In this the input is applied at non-inverting terminal and the inverting terminal is grounded.

→ In this the output is in phase (0° (or) 360°) with the input

→ we know that open loop gain,

$$A = \frac{V_o}{V_d}$$

where, $V_d = V_1 - V_2$

so, $A = \frac{V_o}{V_1 - V_2}$

→ If source resistance R_i is very small, then it is neglected.

$\therefore V_1 = V_i$

$V_o = A(V_i - V_2)$

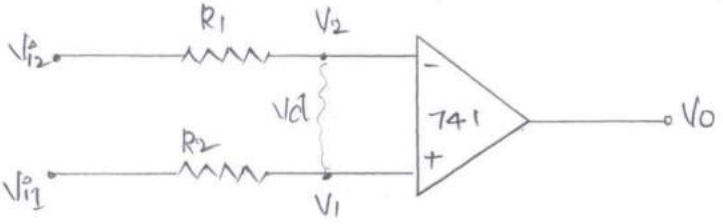
from fig, $V_2 = 0$ ($\because$ it is grounded)

$V_o = A(V_i - 0)$

$\therefore V_o = AV_i$

Where, +ve sign indicates that phase shift is zero provided in input and output.

Differential Amplifier:



→ In this inputs are applied at both the inverting and non-inverting terminals. Since, the difference between two input signals is amplifies which is called Differential Amplifier.

→ We know that open loop gain,

$$A = \frac{V_o}{V_d}$$

Where, $V_d = V_1 - V_2$

So, $A = V_o / V_d$

$$A = \frac{V_o}{V_1 - V_2}$$

$$V_o = A(V_1 - V_2)$$

→ If Source resistance R_i is very Small, then it is neglected

$V_{i1} = V_1$; $V_{i2} = V_2$

So, $V_o = A(V_1 - V_2)$

$\therefore$ $V_o = A(V_{i1} - V_{i2})$

Closed Loop mode of Operation:

In this feed back exist, in between input & output. These feed back is a negative feed back.

→ Due to the negative feed back input resistance increases, output resistance decreases and noise is reduced, band width is increases and gain is decreases.

→ But, op-amp will perform the three basic operation in closed loop mode of operation.

a) Inverting - Amplifier.

b) Non inverting - Amplifier.

c) Differential - Amplifier.

a) Inverting Amplifier:

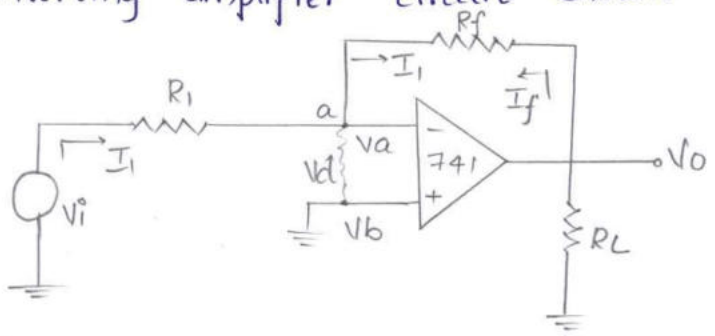
In this inverting input is applied at the inverting terminal and non-inverting terminal is grounded.

→ In this o/p signal is out of phase with the input signal

→ The o/p voltage is fed back to the inverting input terminals through $R_f - R_1$ network.

Where, R_f - feedback resistance

→ The inverting amplifier circuit shown in below figure.



Analysis:

→ Let us assume an ideal op-Amp, $V_d = 0$ and node A is at ground potential (virtual ground) then and I_1 current flows through R_1 resistor.

$$\text{So, } I_1 = \frac{V_A}{R_1} \longrightarrow (1)$$

→ Since, Op-Amp draws no current, all the current flowing with R_1 must flow through R_f resistor. The o/p voltage V_o is given by

$$V_o = -I_i R_f \longrightarrow (2)$$

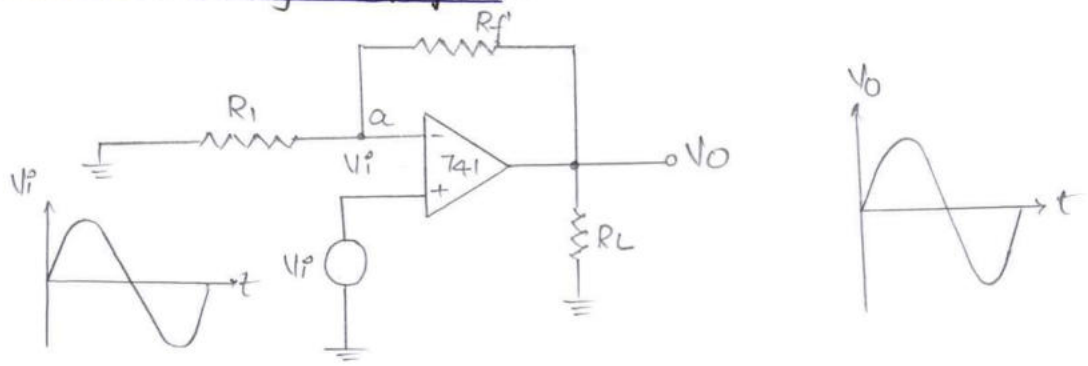
Since on Sub eq (1) & (2), we get

$$V_o = -\frac{V_i}{R_1} \times R_f$$

$$\therefore \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Hence, the closed loop gain of the inverting Amplifier is given by A_{CL}, $A_{CL} = -\frac{R_f}{R_1}$

b) Non-Inverting Amplifier:



→ If a singnal is applied to the non-inverting input teemina then it is called as non-inverting amplifier.

→ If a signal is applied to the non-inverting teemina and feedback is connected from output to input as shown in above figure.

→ It may be noted that it is also a -ve feedback system as output is being fed back to the inverting input terminal.

→ As a differential voltage Vd at the input terminal of Op-amp is zero, the voltage at node 'a' is Vi, same as the input voltage applied to non-inverting input terminal.

→ In circuit Rf and R1 forms a potential divider. Hence, according to procedure potential divider theorem.

$$V_i = \frac{R_1 V_o}{R_1 + R_f}$$

$$V_o = \frac{R_1 + R_f}{R_1} \times V_i$$

$$V_o = 1 + \frac{R_f}{R_1} \times V_i$$

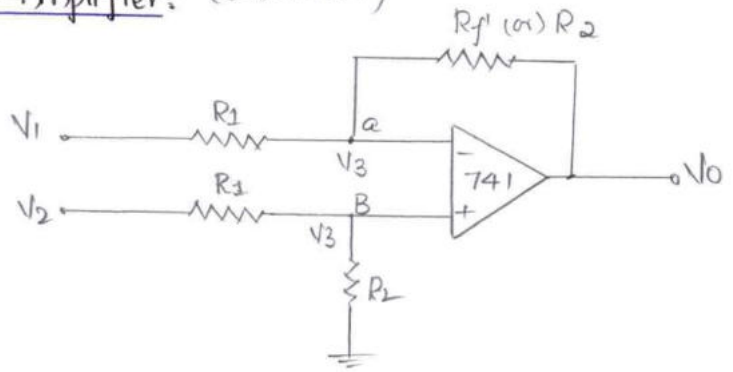
$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

We know that,

$$A_{CL} = \frac{V_o}{V_i}$$

$$\therefore A_{CL} = 1 + \frac{R_f}{R_1}$$

C) Differential Amplifier: (Subtractor)



→ A circuit that amplifies the difference b/w two input signals is called as difference amplifier (or) Differential Amplifier.

→ The differential amplifier circuit is shown in above figure.

→ Since the differential voltage at the input terminal of Op-Amp is zero.

→ Node A and Node B are at the same potential i.e, V_s.

→ The nodal equation at node A is,

$$\frac{V_2 - V_3}{R_1} = \frac{V_s - V_o}{R_2}$$

$$\frac{V_3 - V_2}{R_1} + \frac{V_s - V_o}{R_2} = 0$$

$$V_s\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_2}{R_1} - \frac{V_o}{R_2} = 0 \longrightarrow (1)$$

The nodal equation at node B is,

$$\frac{V_1 - V_3}{R_1} = \frac{V_3}{R_2}$$

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0$$

$$V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_1}{R_1} = 0 \longrightarrow (2)$$

Subtracting the above equations, we get

$$V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] - \frac{V_2}{R_1} - \frac{V_o}{R_2} - V_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right] + \frac{V_1}{R_1} = 0$$

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} - \frac{V_o}{R_2} = 0$$

$$1/R_1 [V_1 - V_2] = V_0/R_2$$

$$\frac{V_0}{V_1 - V_2} = \frac{R_2}{R_1}$$

$$\therefore V_0 = \frac{R_2}{R_1}(V_1 - V_2)$$

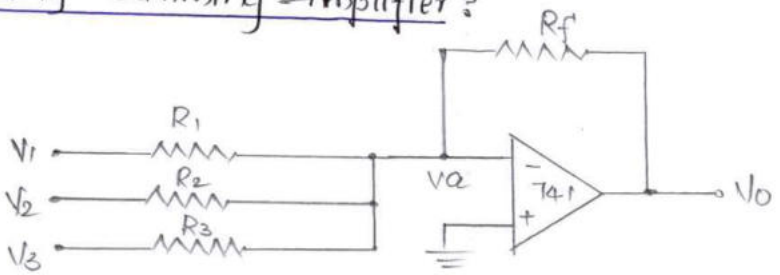
Summing Amplifier:

Op-Amp may be used to design the circuit whose output is the sum of several input signals. Such a circuit is called Summing Amplifier (or) Summer.

→ The summing amplifier are classified into two types.

1. Inverting Summing amplifier.
2. Non-Inverting Summing amplifier.

1. Inverting Summing Amplifier:



→ A typically summing amplifier with 3 i/p voltages V_1, V_2, V_3 & three i/p resistors R_1, R_2, R_3 & one feedback resistor R_f shown in above fig.

→ The voltage at node 'a' is zero ($V_a = 0$) because the non-inverting terminals is grounded.

The nodal equation at node 'a' is given by,

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = \frac{V_a - V_o}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f}$$

$$\frac{V_o}{R_f} = -\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$$

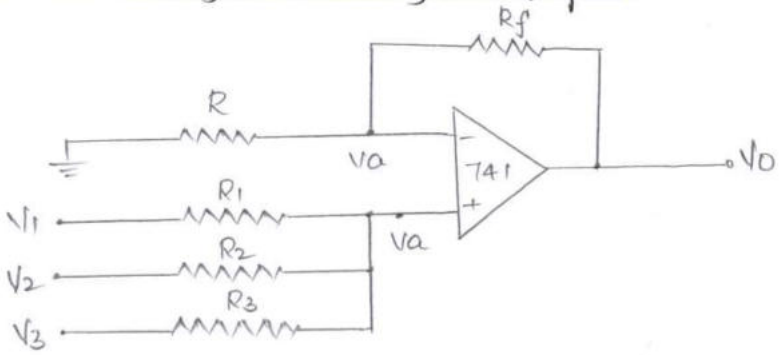
$$V_o = -\left[V_1 \frac{R_f}{R_1} + V_2 \frac{R_f}{R_2} + V_3 \frac{R_f}{R_3}\right]$$

Let, $R_1 = R_2 = R_3 = R_f$

$$\therefore V_o = -[V_1 + V_2 + V_3]$$

Where, -ve sign indicates the phase shift between i/p & o/p. So, it is called as inverting summing amplifier.

2. Non - Inverting Summing Amplifier:



→ The non - inverting summing amplifier shown in above fig.
→ The i/p voltages V_1, V_2, V_3 is fed to the non - inverting terminal. the voltage at non - inverting i/p terminal is 'Va'.
→ The voltage at the inverting i/p terminal will also be Va, because they are virtually grounded.
i.e, The voltage across the inverting terminal is same as that of the non - inverting terminal.

The nodal equation at node 'a' is given by,

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} + \frac{V_2}{R_2} - \frac{V_a}{R_2} + \frac{V_3}{R_3} - \frac{V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_a\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]$$

$$V_a = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}$$

W.k.T gain of non - inverting amplifier is,

$$A = \frac{V_o}{V_d} = 1 + \frac{R_f}{R_1}$$

But Here, $V_d = V_a$

$$V_o = \left[1 + \frac{R_f}{R}\right] \cdot V_a$$

Substitute V_a in above equation,

$$V_o = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{V_1/R_1 + V_2/R_2 + V_3/R_3}{1/R_1 + 1/R_2 + 1/R_3}\right]$$

Let, $R_1 = R_2 = R_3 = R = R_f/2$

$$V_o = \left[1 + \frac{R_f}{R_f/2}\right] \left[\frac{2V_1/R_f + 2V_2/R_f + 2V_3/R_f}{2/R_f + 2/R_f + 2/R_f}\right]$$

$$= 3 \times \frac{2(V_1 + V_2 + V_3)}{6}$$

$$\therefore V_o = V_1 + V_2 + V_3$$

→ Here, the o/p voltage is in phase with sum of the i/p voltages. So, it is called as non-inverting summing amplifier.

Instrumentation Amplifier:

→ measurement of the physical quantities is generally carried out with the help of a device called "Transducer".

→ A transducer is a device which converts one form of energy into another form of energy. Eg: microphone.

→ But most of the transducer o/p are generally very low level signals. Such low level signals are not sufficient to drive the next stage of the op-Amp. Hence, before the next stage it is necessary to amplify the level of such signal, rejecting the noise & interference.

→ However, a general amplifier like a CE amplifier is not suitable to amplify such signals.

→ For rejection of noise, such amplifiers must have high CMRR. But CE amplifier has low CMRR. so, it is not useful. Therefore, a special amplifier is used to amplify such signals.

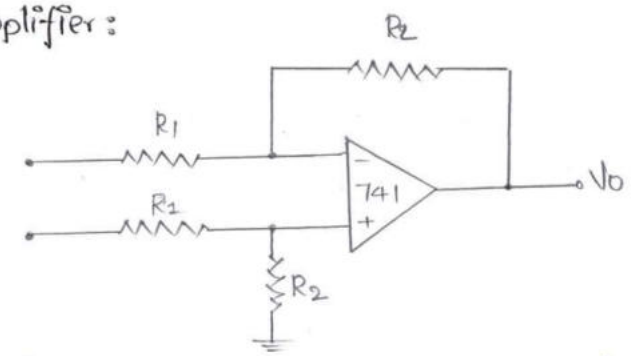
→ A special amplifier which is used for such a low level

amplification with high CMRR, high i/p impedance, low o/p impedance, low power consumption is known as Instrumentation amplifier. It is also called as Data-Amplifier.

→ The requirements of an good instrumentation amplifier is given by:

a) High i/p impedance.
b) Low o/p impedance.
c) High CMRR.
d) Low power consumption.
e) Easier gain adjustment.
f) High slew rate.
g) Gain is high.

Differential Amplifier:

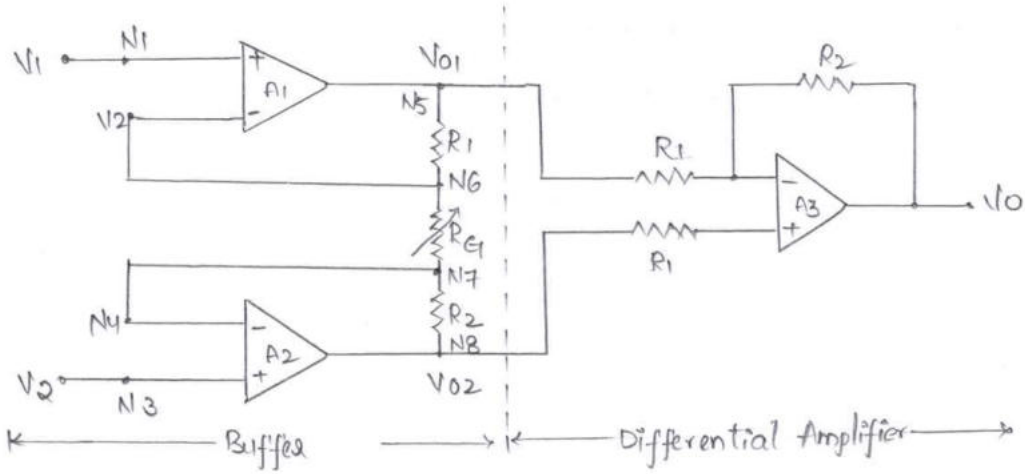


→ The instrumentation amplifier is a type of differential amplifier. Hence, differential amplifier is shown in above fig.

$$\therefore V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

→ The instrumentation amplifier is a type of differential Amplifier i.e, the D.A using op-Amp can be used as instrumentation amplifier. But the main problem in using it as an instrumentation amplifier is its i/p impedance.

→ The i/p impedance of D.A is low while the I.A needs very high i/p impedance. To get very high i/p impedance, the D.A can modified by using Buffer (or) Voltage follower circuit as at the i/p. It is shown in below fig.



→ The gain of the voltage follower circuit is unity. While its i/p impedance is very high. Hence, the circuit provides same voltage gain as provided by the op-amp differential amplifier.

→ It consists of op-amps A1, A2 & A3. Op-amps A1 & A2 are the non-inverting amplifiers forms the i/p stage. Op-amp A3 is differential amplifier forms the o/p stage of the amplifier.

→ Gain depends on the external resistance & hence can be adjusted accurately.

→ The CMRR of the op-amp as is very high. Thus, the current satisfies the all the requirements of a good, instoumentation amplifier & hence commonly used in practical applications.

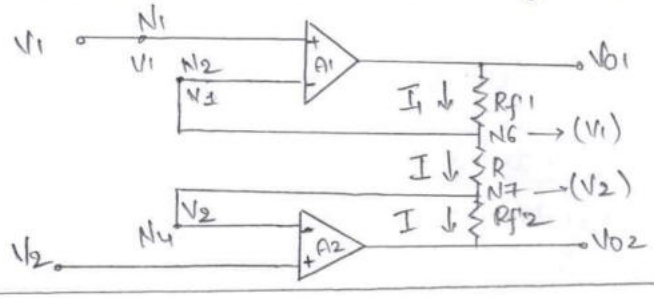
Analysis:

It may be observed that the o/p stage is a basic D.A. Hence, if the o/p of op-amp A1 is V_{01} & o/p of op-amp A2 is V_{02}. So, we can write o/p of op-amp is,

$$\therefore V_o = \frac{R_2}{R_1}(V_{02} - V_{01}) \longrightarrow (1)$$

→ Let us find out the expression for V_{02} & V_{01} in terms of V_1, V_2, R_{f1}, R_{f2}, R.

→ Let us consider the first stage of an I.A shown fig.



→ The node N_1 voltage of op-Amp A_1 is V_1. So, that will be appeared at the node N_2 by virtual ground connection. So the voltage at node N_6 is V_1.

→ The node N_3 voltage of op-Amp A_2 is V_2. So that will be appeared at the node N_4 by virtual connection. So the voltage at node N_7 is V_2.

→ The i/p current of op-Amp of A_1 & A_2 both are zero. Hence, current I remains same through R_{f_1}, R, R_{f_2}.

→ Applying ohms law b/w the nodes N_5 & N_8, we get

$$I = \frac{V_{o1} - V_{o2}}{R_{f_1} + R + R_{f_2}}$$

Let, $R_{f_1} = R_{f_2} = R_f$

So, $$I = \frac{V_{o1} - V_{o2}}{2R_f + R} \rightarrow (2)$$

Now at the nodes N_6 and N_7,

$$I = \frac{V_1 - V_2}{R} \rightarrow (3)$$

Equate eq (2) & (3), we get

$$\frac{V_{o1} - V_{o2}}{2R_f + R} = \frac{V_1 - V_2}{R}$$

multiply '−' on both sides, we get

$$\frac{V_{o2} - V_{o1}}{2R_f + R} = \frac{V_2 - V_1}{R}$$

$$V_{o2} - V_{o1} = \frac{V_2 - V_1}{R}(2R_f + R)$$

$$= V_2 - V_1\left(\frac{2R_f}{R} + \frac{R}{R}\right)$$

$$\therefore V_{o2} - V_{o1} = V_2 - V_1\left(1 + \frac{2R_f}{R}\right) \rightarrow (4)$$

Substitute eq (4) in (1), we get

$$\therefore V_o = \frac{R_2}{R_1}\left(1 + \frac{2R_f}{R}\right)(V_2 - V_1)$$

This is the overall voltage gain of the I.A.

where R is the variable resistor.

∴ The gain is depends on the R.

Applications:

1. Temperature controller.
2. Light intensity meter.
3. Analog weight scale.
4. measure the pressure, weight & humidity.

Ac Amplifier:

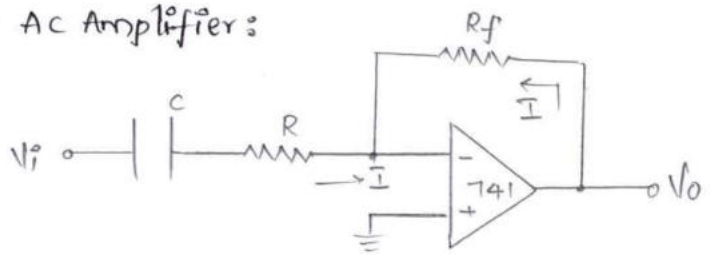
→ The op-amp can amplifies both the types of signals i.e, Dc to Ac. The op-Amp responding to ac signal then it is called as Ac amplifier.

→ If the ac i/p signal is super imposed with the dc signal, to restrict the amplification of such dc signals, the coupling capacitors must be used at the i/p of the ac amplifier.

→ There are 2 types of Ac amplifier:

1. Inverting Ac amplifier.
2. Non-Inverting Ac amplifier.

1. Inverting Ac Amplifier:



→ The above circuit shows the inverting ac amplifier because the Ac i/p signal is fed to the inverting terminals.

→ The capacitor 'c' blocks the dc components and resistor 'R' sets the lower 3dB frequency of amplifier.

→ Since, node 'a' is at ground potential by the virtual connection The o/p voltage vo is given by,

$$\therefore V_o = -IR_f$$

from fig, $$I = \frac{V_i}{R + \frac{1}{j\omega C}}$$

According to Laplace transform

Let, $j\omega = s$

$$\text{So, } I = \frac{V_i}{R + \frac{1}{sC}} \longrightarrow (2)$$

Substitute eq (2) in (1),

$$V_o = -\left[\frac{V_i}{R + \frac{1}{sC}}\right] \times R_f \longrightarrow (3)$$

W.k.T closed loop gain

$$A_{CL} = \frac{V_o}{V_i} \longrightarrow (4)$$

Substitute eq (3) in eq (4)

$$A_{CL} = \frac{-\left(\frac{V_i}{R + 1/sC}\right) R_f}{V_i} = \frac{-1}{R + 1/sC} \times R_f$$

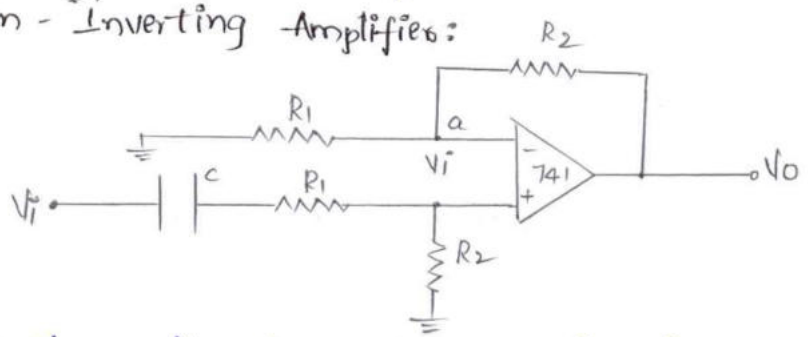
$$= -\frac{R_f}{R}\left[\frac{1}{1 + \frac{1}{sRC}}\right] = \frac{-R_f}{R}\left[\frac{1}{1/s\,(s + 1/RC)}\right]$$

$$\therefore A_{CL} = -\frac{R_f}{R}\left[\frac{s}{s + 1/RC}\right]$$

The capacitor 'c' is short circuited for mid frequencies. So, the 2nd term in the above equation becomes unity.

$$\therefore A_{CL} = \frac{-R_f}{R}$$

2. Non - Inverting Amplifier:



The above fig. shows the non - inverting Ac amplifier because of the i/p Ac signal is fed to the non - inverting terminal. The o/p voltage vo is given by,

$$\therefore V_o = 1 + \frac{R_2}{R_1}$$

Voltage - Current Convertor:

→ In V-I convertor the o/p load current is proportional to the i/p voltage.

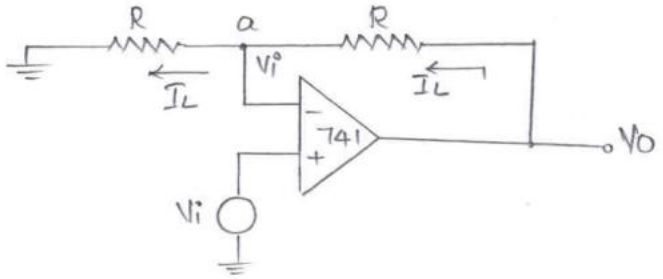
→ According to connection of load there are 2 types:
1. Floating type V-I convertor.
2. Grounded type V-I convertor.

→ In floating type V-I convertor, the load resistor R_L is not connected to the ground.

→ In grounded type V-I convertor, the load resistor R_L is directly connected to the ground.

→ This circuit is also called as voltage controlled current source.

1. Floating Type V-I Convertor:



→ The above fig. shows the V-I convertor. Here, the load resistor R_L is not connected to the ground.

Since, the voltage at node 'a' is $V_i = I \cdot R$

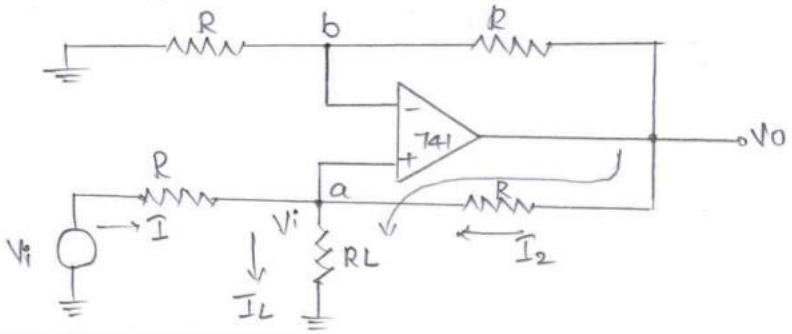
$$\therefore I_L = \frac{V_i}{R}$$

→ Thus, the load current is directly proportional to the i/p voltage and it is given by,

$$\therefore I_L \propto V_i$$

Therefore, this circuit is called Transconductance amplifier.

2. Grounded Type V-I Convertor:



→ A V-I convertor with grounded load is shown in above fig.

→ Let V_1 be the voltage at node 'a' applying KCL at node 'a'.

we get $I_1 + I_2 = I_L \longrightarrow (1)$

from fig. $I_1 = \frac{V_i - V_1}{R_1} \longrightarrow (2)$

$$I_2 = \frac{V_0 - V_1}{R} \longrightarrow (3)$$

Substituting eq (2) & eq (3) in eq (1)

$$\frac{V_i - V_1}{R} + \frac{V_0 - V_1}{R} = I_L$$

$$V_i - V_1 + V_0 - V_1 = I_L \cdot R$$

$$V_i - 2V_1 + V_0 = I_L \cdot R$$

$$\therefore V_1 = \frac{V_i + V_0 - I_L \cdot R}{2} \longrightarrow (4)$$

W.k.T, $A = \frac{V_0}{V_1} = 1 + \frac{R_f}{R}$

But Here, we have $R_f = R$

$$\frac{V_0}{V_1} = 1 + \frac{R}{R} = 2$$

$$\therefore V_0 = 2V_i \longrightarrow (5)$$

Substituting eq (4) in eq (5)

$$V_0 = \frac{2(V_i + V_0 - I_L \cdot R)}{2}$$

$$V_0 = V_i + V_0 - I_L \cdot R$$

$$V_i = I_L \cdot R$$

$$\therefore I_L = \frac{V_i}{R}$$

→ From the above equation, we can say that the load current I_L depends on the i/p voltage V_i.

$$\therefore I_L \propto V_i$$

Applications:

1. Low voltage to dc voltage convertor
2. Diode tester.
3. Zener diode tester.

Current - Voltage Convertor:

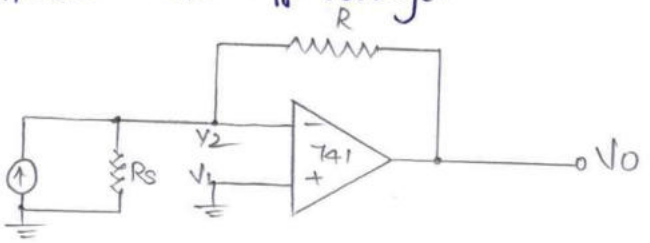
→ In I-V convertor the o/p voltage is directly proportional to the i/p current.

$$V_o \propto I_s$$

where, V_o = o/p voltage

I_s = i/p current

→ This circuit is also called as current controlled voltage source because the o/p voltage controlled by the i/p current (or) i/p current controls the o/p voltage.



→ The above fig. shows the current to voltage convertor because of virtual ground the voltage $V_2 = 0$.

Applying KCL at node 'a'.

$$I_s = \frac{V_2 - V_o}{R}$$

$$V_2 = 0$$

$$I_s = \frac{-V_o}{R}$$

$$\therefore V_o = -I_s R$$

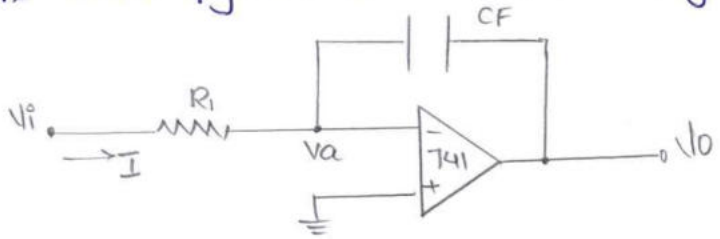
→ Thus the o/p voltage is proportional to the i/p current. So the current works as current to voltage convertor. It is also called as Transresistance amplifier.

Applications:

1. photo diode detectors
2. photo Fet detectors.

Integrator:

Integrator is a circuit in which o/p voltage is integral of i/p voltage. The below fig. shows the ideal integrator circuit.



→ The i/p voltage V_i as applied to the inverting i/p terminal through R_1 resistor.

→ The capacitor current I is given by $I = C_F \frac{dv}{dt}$.

→ Since, o/p current of op-amp is zero, the entire current I flowing through R_1 & C_F.

Applying KCL at node 'a'.

For i/p side of $I = \frac{V_i - V_a}{R_1}$

where, $V_a = 0V$; because virtual connection.

$$I = \frac{V_i}{R_1} \rightarrow (1)$$

At o/p side, $I = C_F \frac{d(V_a - V_o)}{dt}$

$$I = -C_F \frac{dv_o}{dt} \rightarrow (2)$$

equating eq (1) & eq (2)

$$\frac{V_i}{R_1} = -C_F \frac{dv_o}{dt}$$

$$dv_o = \frac{-v_i dt}{R_1 C_F}$$

integrator on b.s, we get

$$\int_0^t dv_o = \frac{-1}{R_1 C_F} \int_0^t v_i(t)\,dt$$

$$V_o(t) - V_o(0) = \frac{-1}{R_1 C_F} \int_0^t v_i(t)\,dt$$

$$V_o(t) = \frac{-1}{R_1 C_F} \int_0^t v_i(t)\,dt + V_o(0)$$

where, $R_1 C_F = \tau$ = Time constant of integrator

$V_o(0)$ is the initial o/p voltage.

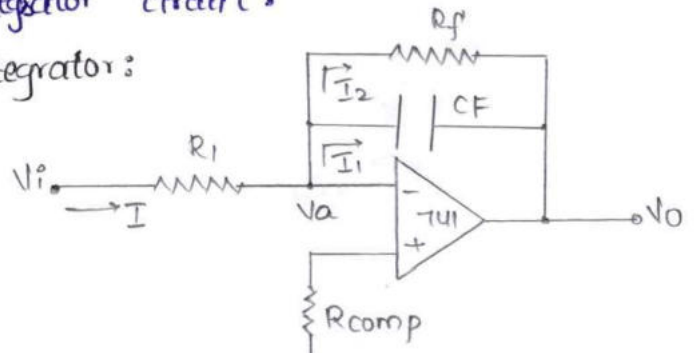
→ The above equation shows that the o/p is $\frac{-1}{R_1 C_F}$ times the integral of i/p.

Drawbacks:

1. Without giving any i/p, we get some voltage at the o/p. So we can treat that as error signal.
2. Capacitor gets charging & discharging due to bias current & add its effects on o/p error voltage. After some time o/p of op-amp may achieve its saturation level.
3. Band-width is very small for ideal integrator. Hence, ideal integrator can be used for very small frequency range of i/p's only.

→ Because of all the above draw backs the ideal integrators is not used in practically. Some additional components are used along with basic integrator circuit to reduce the effect of an error voltage in practically such an integrator is called as practical integrator circuit.

Practical Integrator:



→ The draw back of an ideal integrator can be minimised in the practical integrator circuit, which consists of resistance R_F in parallel with the capacitance C_F.

→ The practical integrator circuit shown in above fig.

→ The resistance Rcomp is used to over come the errors due to the bias currents.

→ The resistance R_f reduces the low frequency gain of the op-amp.

→ The parallel combination of R_f & C_f behaves like a practical capacitor. For this reason this circuit is also called as "Lossy Integrator".

→ Since, i/p current of op-amp is zero, from the concepts of virtual ground $V_a = 0$.

Applying KCL at node 'a',

$$I = I_1 + I_2 \longrightarrow (1)$$

But, $I = \frac{V_i - V_a}{R_1}$

$$I = \frac{V_i}{R_1} \longrightarrow (2)$$

$$I_1 = -C_F \frac{dv_o}{dt} \longrightarrow (3)$$

$$I_2 = \frac{-V_o}{R_f} \longrightarrow (4)$$

Substitute eq (2) & (3) & (4) in eq (1),

$$\frac{V_i}{R_1} = -C_F \frac{dv_o}{dt} - \frac{V_o}{R_f}$$

Apply L.T on both sides, we get

$$\frac{V_i(s)}{R_1} = -C_F \frac{dv_o}{dt} - \frac{V_o(s)}{R_f}$$

$$\frac{V_i(s)}{R_1} = -V_o(s)\left[sC_F + \frac{1}{R_f}\right]$$

$$V_o(s) = \frac{-V_i(s)}{R_1\left[sC_F + 1/R_f\right]}$$

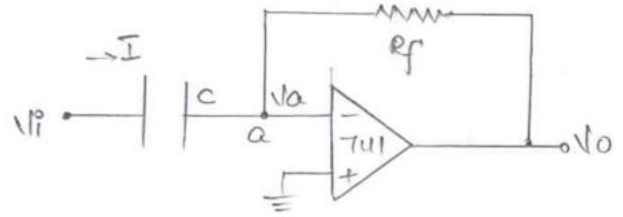
$$\therefore \quad V_o(s) = \frac{-V_i(s)}{sC_1R_1 + R_1/R_f}$$

Applications:

1. It is used in Analog computers.
2. Analog-to Digital convertors.
3. Solving differential equations.
4. Wave shapping circuits.

Differentiator:

Differentiator is a circuit in which o/p voltage is differentiate d to i/p voltage. The below fig. shaos the ideal differentiator.



The node 'a' is at virtual ground potential i.e, $V_a = 0$.

→ The current I flowing through the capacitor is

$$I = C \frac{dv}{dt}$$

→ Apply KCL at node 'a'

$$I = C \frac{d(v_i - v_a)}{dt}$$

Due to virtual connection $V_a = 0$

$$I = C \frac{dv_i}{dt} \rightarrow (1)$$

Similarly at the o/p side

$$I = \frac{V_a - V_o}{R_f} = \frac{-V_o}{R_f} \rightarrow (2)$$

Equating above 2 equations,

$$C \frac{dv_i}{dt} = \frac{-V_o}{R_f}$$

$$\therefore V_o = -R_f \cdot C \frac{dv_i}{dt}$$

Where, $R_f.C$ = Time constant

→ Thus, the o/p voltage vo is constant $(-R_f.C)$ theme the derivative of the i/p voltage.

Draw backs:

1. The gain of the differentiator increases as frequency increases. Thus at some high frequency the differentiator may become unstable & break into the oscillations.
2. The i/p impedance $X_{C_1} = \frac{1}{2\pi f C}$. if frequency increases impedance

decreases. This makes circuit very much sensitive to noise.

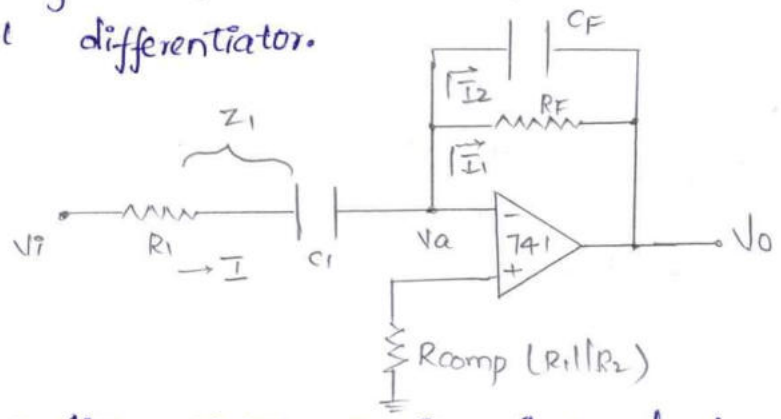
3. Thus, noise may completely overwrite the o/p of the differentiator.

Hence, the differentiator circuit suffers from the stability & noise problem at high frequencies.

→ These problems can be overcome by adding additional components.

Practical Differentiator:

→ The differentiator circuit suffers from the stability & noise problems at high frequencies. These problems can be eliminated by practical differentiator.



→ The practical differentiator circuit designed by using resistance R_1 is in series with C_1 & capacitor C_f is in parallel with resistance R_f.

→ The resistance Rcomp is used for bias compensations.

Analysis:

→ The current I flowing through the R_1 & C_1 components. But the series combination of R_1 & C_1 is denoted by impedance Z_1.

$$\text{So, } I = \frac{V_i}{Z_1}$$

According to L.T,

$$I = \frac{V_i(s)}{Z_1} \longrightarrow (1)$$

W.k.T, $Z_1 = R_1 + \frac{1}{j\omega C_1}$

$$Z_1 = R_1 + \frac{1}{sC_1}$$

$$\therefore Z_1 = \frac{R_1 s C_1 + 1}{s C_1}$$

Substituting Z_1 in eq ①, we get

$$I = \frac{V_i(s)\, s C_1}{R_1 s C_1 + 1}$$

Similarly, $I_1 = \frac{-V_o}{R_f}$

$$I_2 = -C_F \frac{dv_o}{dt}$$

$$\therefore I_1 = \frac{-V_o(s)}{R_f}$$

$$\therefore I_2 = -s C_F V_o(s)$$

Applying KCL at node 'a'

$$I = I_1 + I_2$$

$$\frac{V_i(s)\, s C_1}{1 + R_1 s C_1} = \frac{-V_o(s)}{R_f} - s C_f V_o(s)$$

$$= -V_o(s) \left[\frac{1}{R_f} + s C_f \right]$$

$$= -V_o(s) \left[\frac{1 + s C + R_f}{R_f} \right]$$

$$\therefore V_o(s) = \frac{-V_i(s)\, s C_1 R_f}{(1 + s C_1 R_1)(1 + s C_f R_f)}$$

Let us assume $R_f C_f = R_1 C_1$

$$V_o(s) = \frac{-V_i(s)\, s C_1 R_f}{(1 + s C_f R_f)^2}$$

If $R_f C_1 > C_f R_f$, then the denominator can be neglected.

$$\therefore V_o(s) = -V_i(s)\, s C_1 R_f$$

By applying inverse L.T to the above equation, we get

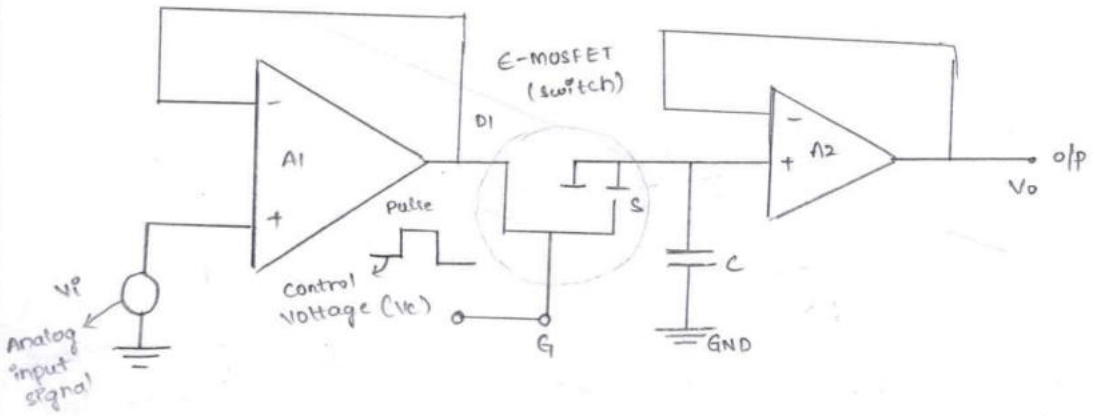
$$\therefore V_o(t) = -R_f C_1 \frac{dv_i(t)}{dt}$$

Applications:

1. It is used in wave shaping circuits.
2. It is used in convertors i.e, analog to digital.

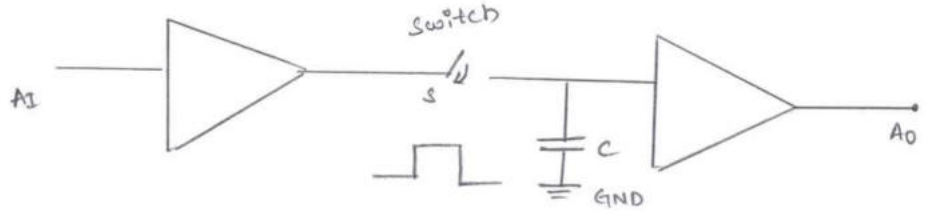
Non-linear application of op-Amp:

Sample and Hold circuits;

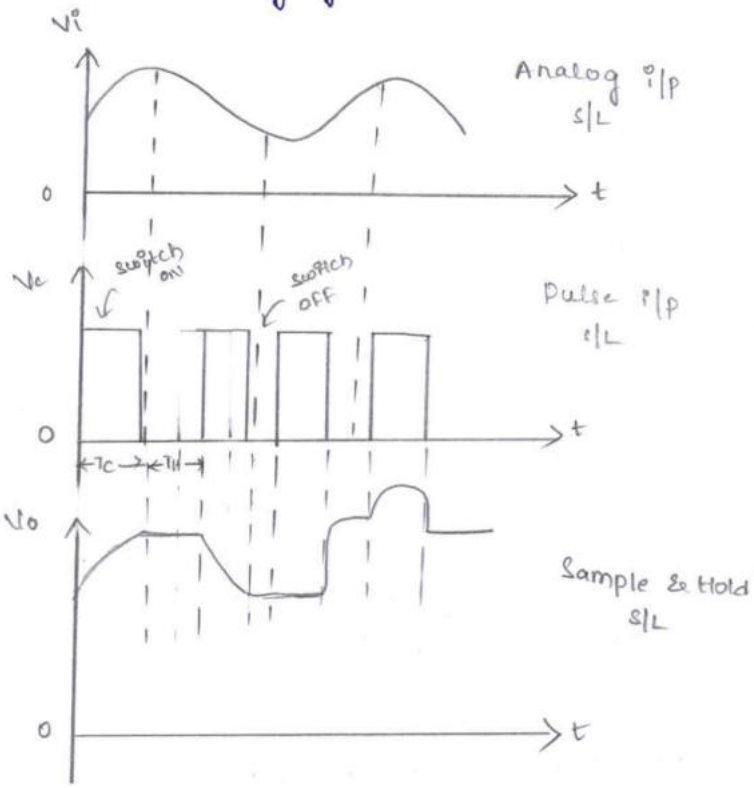


- Sample hold circuit is a circuit in which samples the i/p signal and holds on to its last sampled value until the o/p is sampled again.
- This type of circuit is very useful in analog to digital convertors and digital communications etc
- The above fig E-MOSFET acts as switch & is controlled by the control voltage Vc & capacitor 'c' stores the charge
- The analog signal Vi to be sampled is applied at the non-inverting terminal of A1 op-amp & the same vtg appeared at the drain terminal of E-MOSFET. when the control voltage Vc is applied to its gate. the +ve half cycle is going, the MOSFET is ON which acts as a closed switch & the capacitor 'c' charged by the i/p voltage Vi and the same voltage appears at the o/p of the op-amp
- when -ve half cycle is going the MOSFET is switched off and only discharge path for capacitor c through non-inverting i/p of the op-amp.
- Since the i/p impedance of the op-amp is high, the voltage Vi is retained & this appears at the o/p of the op-Amp

- The i/p & o/p waveforms of the circuit shown in below fig



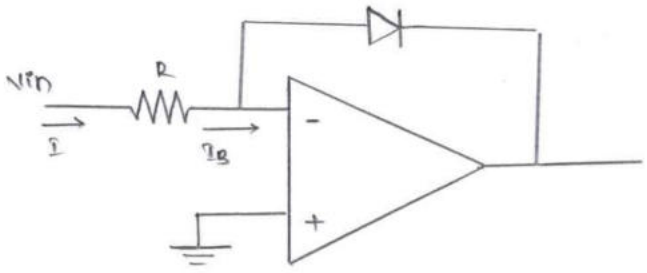
- The time period of the signal during which the voltage across the capacitor (Vc) is equal to Vi is called Sample period (T_S) (or) on time (or) charging time
- The time period of the signal during which the voltage across the capacitor Vc is held constant are called Hold period (T_H) (or) off time (or) Discharging time
- The time period of the signal during which the voltage across the capacitor Vc is held constant are called hold period (T_H) or off time (or) Discharging time.



Log amplifier

A logarithmic amplifier, or a log amplifier, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input

An op amp based logarithmic amplifier produces a voltage at the output, which is proportional to the logarithm of the voltage applied to the resistor connected to its inverting terminal.



$$I = I_B + I_D$$

$$I = I_D$$

$$\frac{V_{in}}{R} = I_s \left(e^{V_d/\eta V_T}\right)$$

$$= \frac{V_{in}}{RI_s} e^{V_d/\eta V_T}$$

$$V_d = 0 - V_{out} = -V_{out}$$

$$\frac{V_{in}}{RI_s} = e^{-V_{out}/\eta V_T}$$

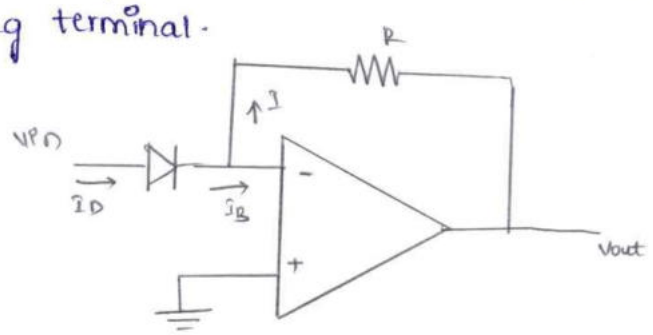
log on both sides $[\log A^B = B \log A]$

$$V_{out} = -\eta V_T \log\left(\frac{V_{in}}{RI_s}\right)$$

Antilog-logarithmic amplifier:

An anti-logarithmic amplifier or an anti-log amplifier, is an electronic circuit that produces an output that is proportional to the anti logarithm of the applied input.

An op-amp based anti-logarithmic amplifier produces a voltage at the output, which is proportional to the anti-logarithmic of the voltage that is applied to the diode connected to its inverting terminal.



By applying KCL,

$$I_D = I$$

$$I_D = I_s \left(e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

$$= I_s \left(e^{V_D/\eta V_T} >> 1 \right)$$

$$I_D = I_s e^{V_D/\eta V_T}$$

$$I = \frac{-V_{out}}{R}$$

$$I_s e^{\frac{V_D}{\eta V_T}} = \frac{-V_{out}}{R}$$

$$V_D = V_{in}$$

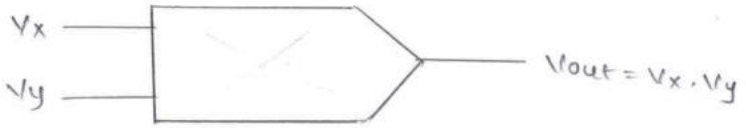
$$I_s e^{V_{in}/\eta V_T} = \frac{-V_{out}}{R}$$

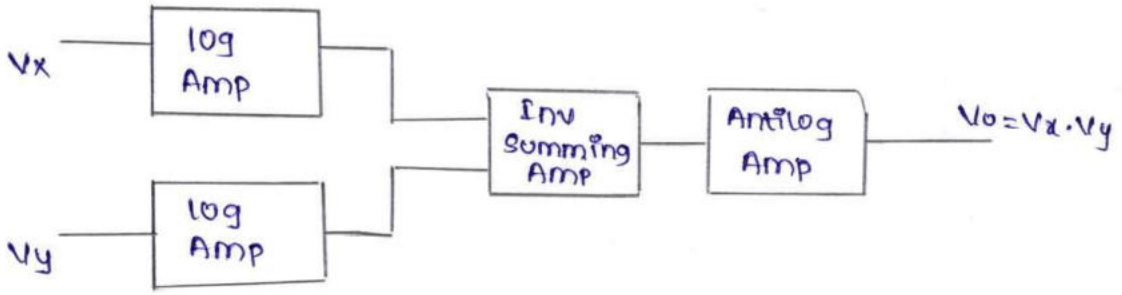
$$\boxed{V_{out} = -I_s R e^{V_{in}/\eta V_T}}$$

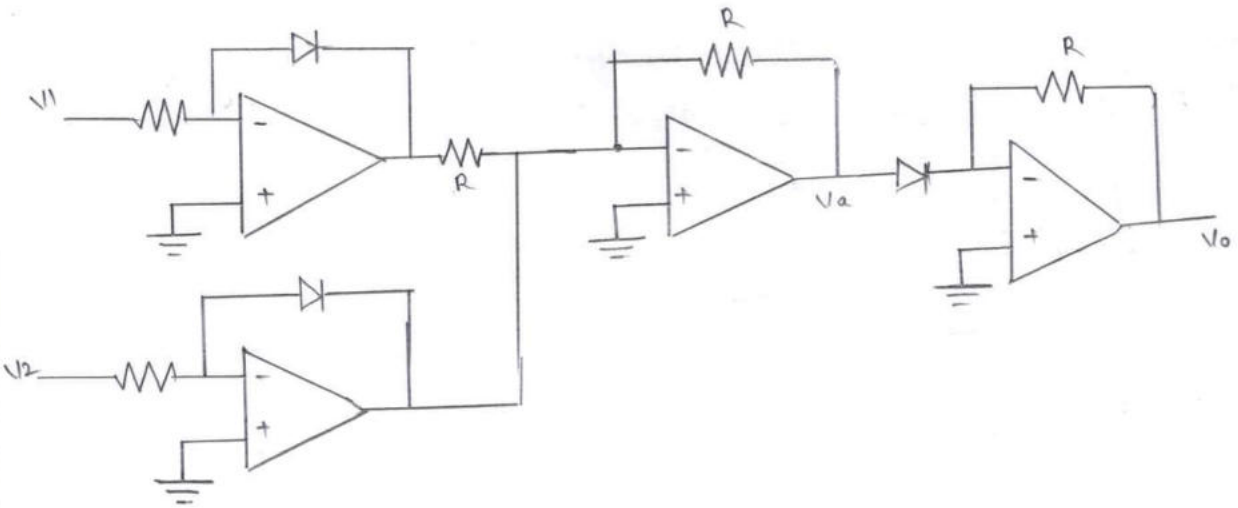
Analog multiplier:

In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. such circuits are termed analog multipliers

- Hence analog multiplier is a circuit in which the output voltage is proportional to multiplication of input voltages







$$V_o = \eta V_T \log \frac{V_{in}}{I_s R}$$

$$V_{o1} = -\eta V_T \log \frac{V_1}{I_s R}$$

$$V_{o2} = -\eta V_T \log \frac{V_2}{I_s R}$$

$$V_a = -(V_{o1} + V_{o2})$$

$$= -\left(-\eta V_T \log \frac{V_1}{I_s R} - \eta V_T \log \frac{V_2}{I_s R}\right)$$

$$V_a = \eta V_T \left(\log \frac{V_1}{I_s R} + \log \frac{V_2}{I_s R}\right)$$

$$= \eta V_T \log \frac{V_1 V_2}{I_s^2 R^2} \quad -①$$

$$V_o = -I_s R\, e^{\frac{V_{in}}{\eta V_T}}$$

$$V_o = -I_s R \text{ antilog } \frac{\eta V_T \log \frac{V_1 V_2}{I_s^2 R^2}}{\eta V_T}$$

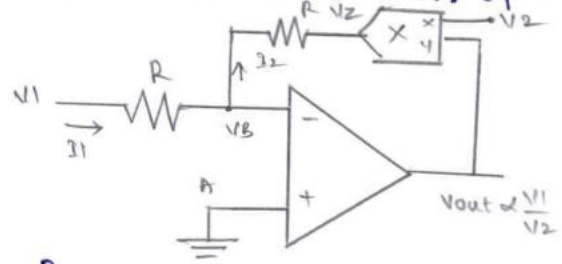
$$= -I_s R \frac{V_1 V_2}{I_s^2 R}$$

$$\boxed{V_o = -K V_1 V_2} \qquad K = \frac{1}{I_s R}$$

$V_o \propto V_1 V_2$

Analog divider:

Analog divider is a circuit in which the output voltage is proportional to division of input voltages



By applying KCl at node B

$$I_1 = I_2$$

$$\frac{V_1 - V_B}{R} = \frac{V_B - V_Z}{R} \quad -①$$

By virtual GND concept $V_A = V_B = 0$

$$V_1 = -V_Z$$

$$V_Z = K V_2 V_o$$

$$V_1 = -K V_2 V_o$$

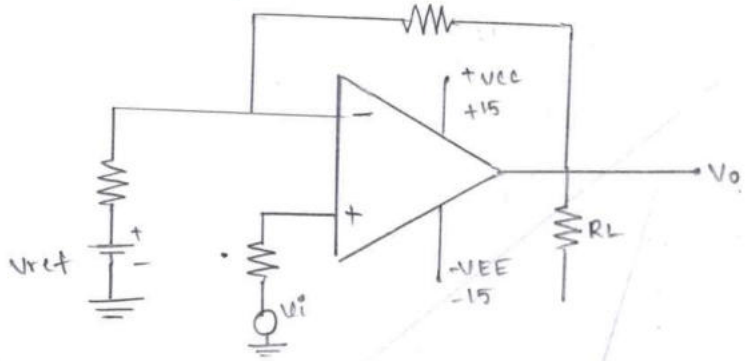
$$V_o = \frac{V_1}{-K V_2}$$

$$\boxed{V_o \propto \frac{V_1}{V_2}}$$

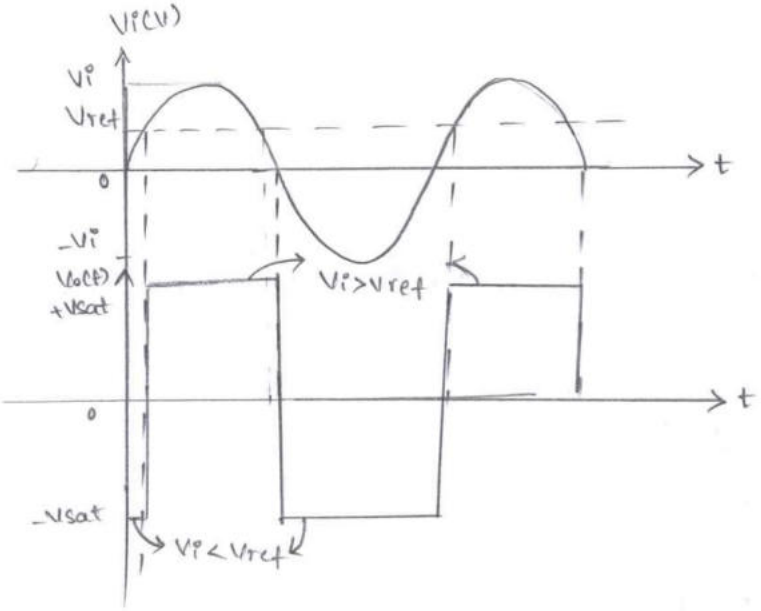
Comparator:

- Comparator is a circuit in which compares the signal voltage at one i/p terminal of an op-amp with a known reference voltage at another i/p terminal of an op-amp
- Basically comparators are of 2 types
  1) Non-inverting comparator
  2) Inverting comparator

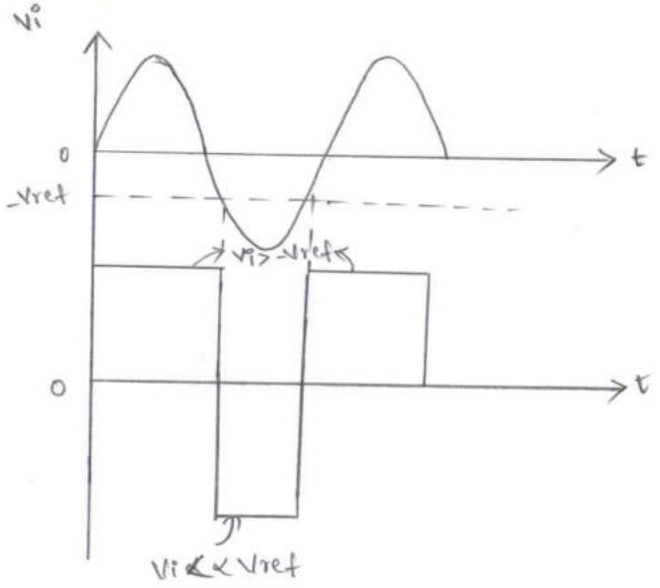
1) Non-Inverting comparator:



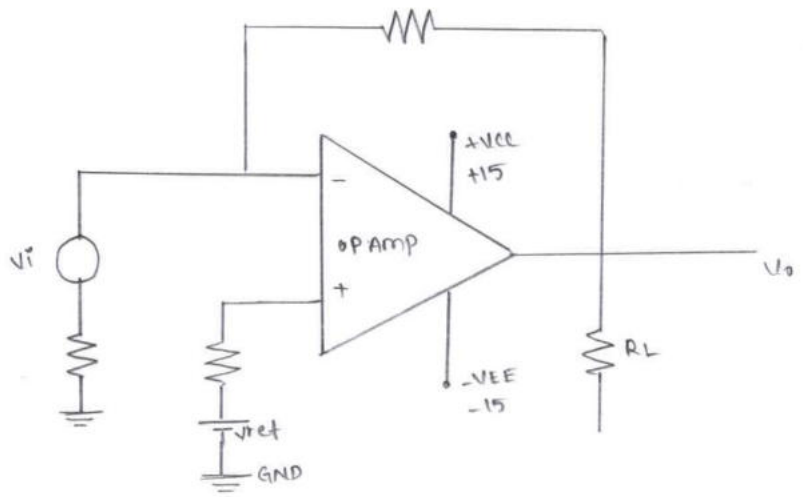
- The above fig shows the non-inverting comparator.
- A fixed reference voltage Vref is applied to the inverting i/p terminal & signal voltage Vi is applied to the non-inverting i/p terminal
- Because of this arrangement the circuit is called non-inverting comparator
- when $V_i < V_{ref}$, the o/p voltage V_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the inverting i/p terminal (-ve i/p terminal) is higher than that of non-inverting i/p terminal (+ve i/p terminal)
- Similarly when $V_i > V_{ref}$, the +ve i/p voltage is greater than the -ve i/p voltage. So o/p voltage V_o goes to $+V_{sat}$ ($\cong +V_{CC}$)
- Thus o/p voltage V_o changes from one saturation level to another saturation level whenever $V_i = V_{ref}$, the corresponding i/p & o/p waveforms for +ve reference Vtg is shown in fig



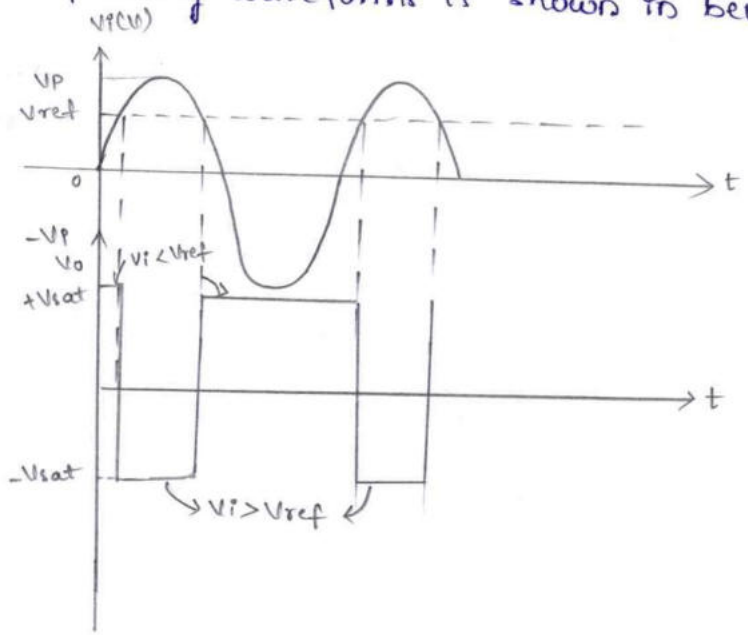
- If the reference voltage Vref is -ve with respect ground with the signal applied to the +ve terminal
- The corresponding waveforms are shown below

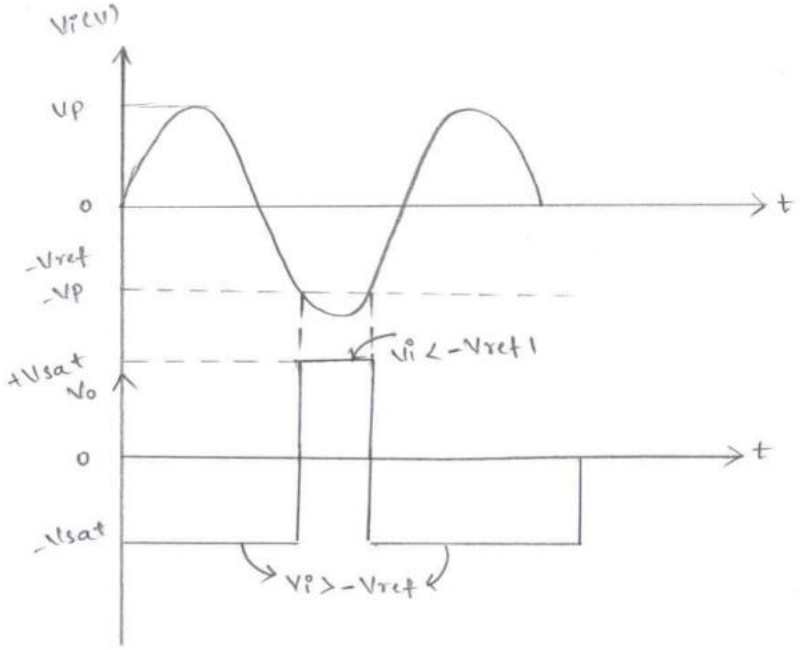


Inverting comparator:



- It is a circuit in which the reference voltage Vref is applied to non-inverting terminal & signal voltage is applied to the inverting terminal
- when $V_i < V_{ref}$, the o/p voltage V_o is at $+V_{sat}$ ($+V_{CC}$), because the voltage at the inverting input is less than that the non-inverting i/p voltage
- Similarly when $V_i > V_{ref}$, the non-inverting i/p is less than the inverting i/p then V_o goes to $-V_{sat}$ ($-V_{EE}$)
- The corresponding waveforms is shown in below



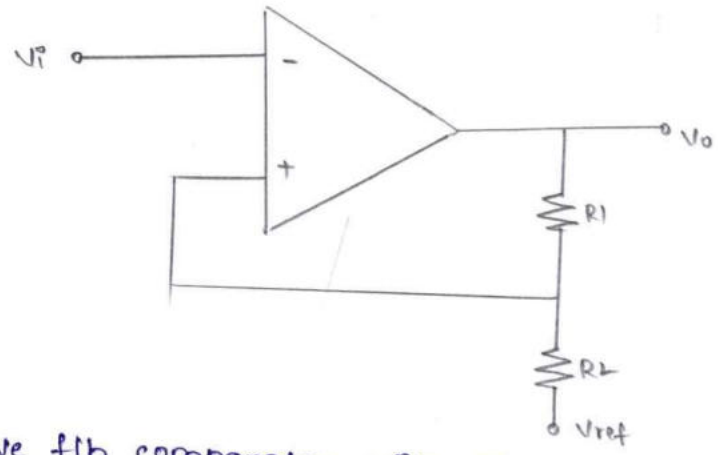


Application:

1) Zero crossing detector
2) Schmitt trigger (regenerative comparator)

Schmitt trigger:

- In basic comparator circuit f/b is not used & op-amp is used in open loop mode
- In open loop op-amp gain is large. At any cost where small noice voltage can cause triggering of the comparator such unwanted noise cause the o/p to jump b/w high & low state
- The comparator circuit used to avoid such unwanted triggering (change) is called regenerative comparator (or) schmitt trigger which basically uses +ve f/b
- A comparator circuit with +ve f/b is known as schmitt trigger (or) regenerative comparator.



- A +ve f/b comparator with signal is applied at -ve i/p is shown in above fig
- The i/p voltage Vi triggers the o/p voltage Vo everytime it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) & lower threshold voltage (V_{LT})
- The difference b/w these voltages are called hysteresis voltage (V_H)

$$\therefore V_H = V_{UT} - V_{LT}$$

- The threshold voltages are calculated as follows

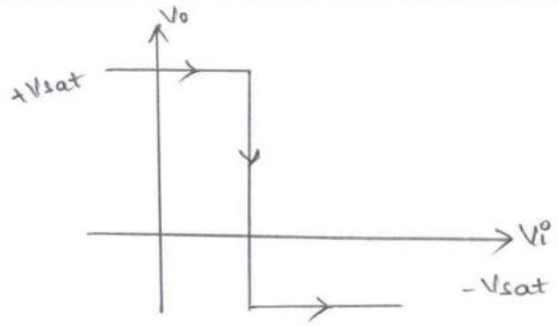
a) Suppose o/p voltage $V_o = +V_{sat}$, the voltage at +ve i/p terminal can be obtained by using super position theorem

$$V_{UT} = \frac{V_{ref} \cdot R1}{R1+R2} + \frac{V_{sat}\, R2}{R1+R2}$$

These voltage is called upper threshold voltage (V_{UT})

b) if $V_i < V_{UT}$, the o/p V_o remains constant at $+V_{sat}$

c) when V_i is just greater V_{UT}, the o/p regeneratively switches to $-V_{sat}$ & remains at this level until $V_i > V_{UT}$



d) for $V_o = -V_{sat}$, the voltage at +Ve i/p terminal is

$$V_{LT} = \frac{V_{ref} \cdot R1}{R1+R2} \cdot -\frac{V_{sat} R2}{R1+R2}$$

This voltage is called lower threshold voltage

e) The i/p voltage is Vi must become lesser than V_{LT} in order to cause V_o to switch from $-V_{sat}$ to $+V_{sat}$

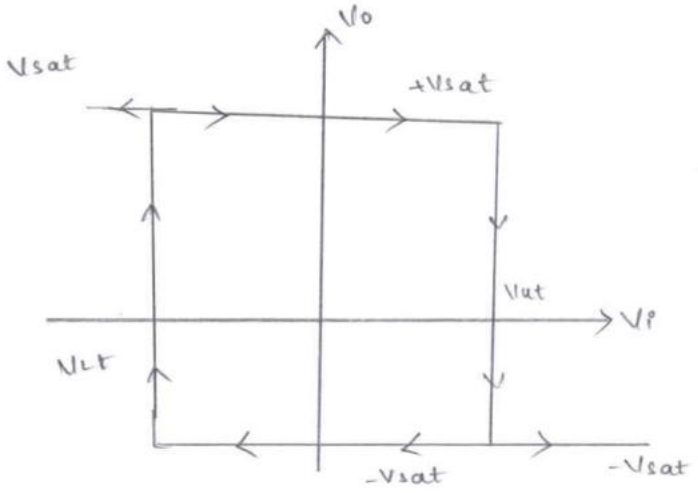
f) A regenerative transiction takes place & o/p V_o returns from $-V_{sat}$ to $+V_{sat}$, shown in below fig

g) The difference b/w 2 threshold voltage called as hysteresis voltage V_H

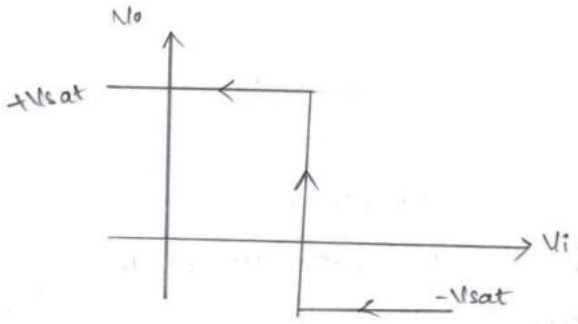
$$V_H = V_{UT} - V_{LT}$$

$$= \frac{V_{ref} R1}{R1+R2} + \frac{V_{sat} \cdot R2}{R1+R2} - \frac{V_{ref} R1}{R1+R2} + \frac{V_{sat} \cdot R2}{R1+R2}$$

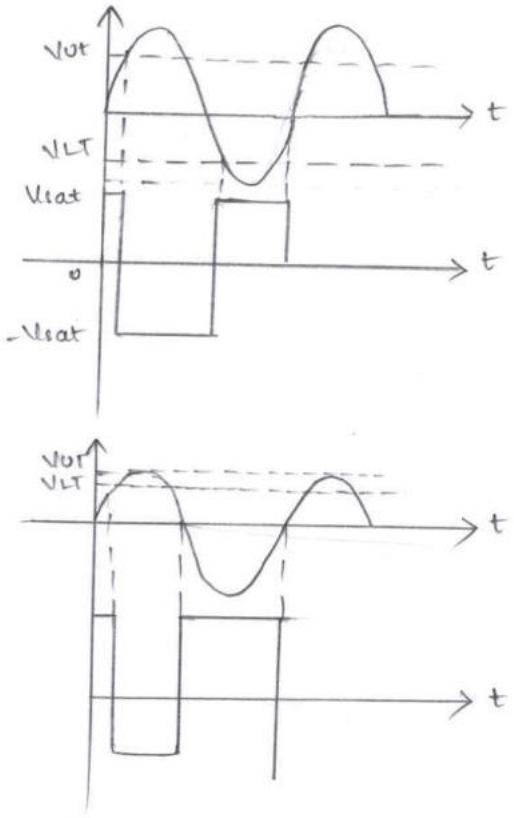
$$V_H = \frac{2 V_{sat} \cdot R2}{R1+R2}$$



h) The hysteresis curve is shown in below fig



- corresponding i/p & o/p waveform, of schmitt trigger shown in fig



Active filters:

Introduction:

- Filter is a frequency selective device. It is a circuit which is used for selecting a particular band of frequency.
- Filter can be designed which passive and as well as the active components
- Passive elements are resistance, capacitor & inductor
- If the circuit designed with RLC which is called passive filter
- Active elements are transistors, op-amps. If the circuit is designed with op-amp which is called as active filter
- In active filter resistors and capacitors are also be used to desire circuit.
- RC filters are used for low frequency oscillators. LC filters are used for high frequency oscillators

Advantages of active (or) passive filters:

1) Gain and frequency adjustment flexibility

2) No loading effect

3) It is cheap (It is the cost is very low)

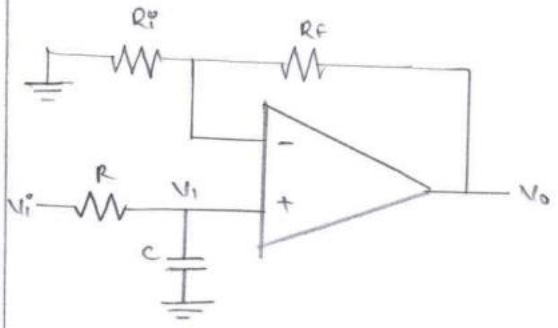
4) The most commonly used filters are

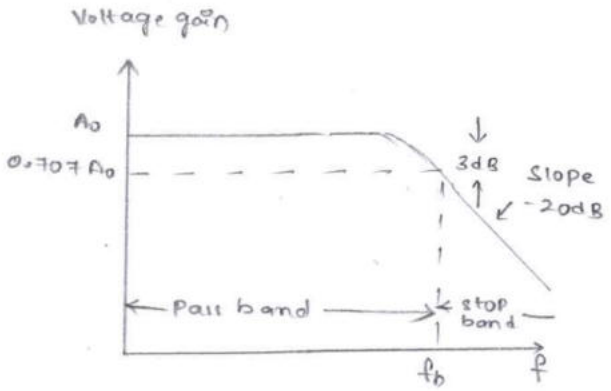
   a) Low pass filter (LPF)
   b) High pass filter (HPF)
   c) Band pass filter (BPF)
   d) Band reject filter (BRF)
   e) All pass filter.

Butterworth filters:

Butterworth filters is type of frequency response in which has constant pass band and constant stop band.

First order low pass filter:





The voltage V_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

$$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs+1}$$

where V(s) is the laplace transform of v in time domain

The closed loop gain Ao of the op-amp is

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_i}\right)$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \times \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs+1}$$

Let $\omega_h = \frac{1}{RC}$

Therefore, $H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{\frac{s}{\omega_h}+1} = \frac{A_o\omega_h}{s+\omega_h}$

This is the standard form of the transfer function of a first order low pass system.

To determine the frequency response, put $s = j\omega$

$$H(j\omega) = \frac{A_0}{1+j\omega RC} = \frac{A_0}{1+j(f/f_h)}$$

where $f_h = \frac{1}{2\pi RC}$ and $f = \frac{\omega}{2\pi}$

At very low frequency, i.e $f << f_h$

$$|H(j\omega)| \simeq A_0$$

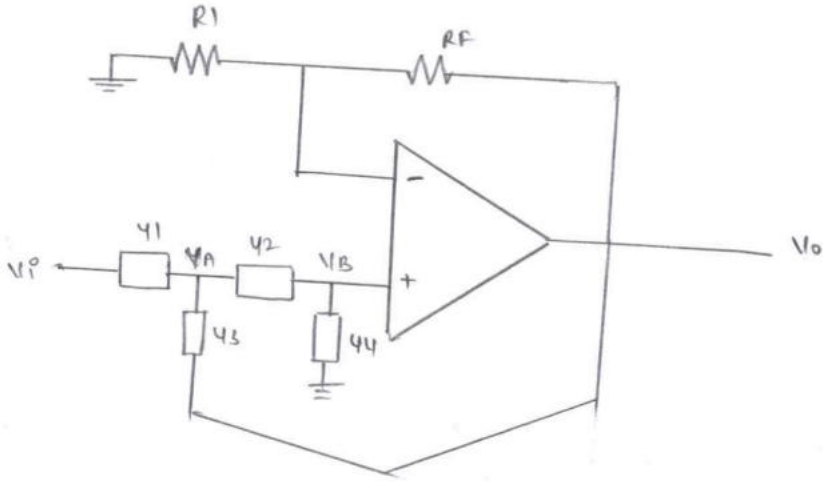
$f = f_h$,

$$|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0$$

At very high frequency i.e $f >> f_h$

$$|H(j\omega)| << A_0 \simeq 0$$

Second order active filter:



$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_B \quad -①$$

$$V_o = A_o V_B$$

$$V_B = \frac{V_o}{A_o} \quad -②$$

By applying KCL at node A

$$(V_i - V_A)\,y_1 = (V_A - V_B)\,y_2 + (V_A - V_o)\,y_3$$

$$V_i y_1 = V_A y_1 + V_A y_2 - V_B y_2 + V_A y_3 - V_o y_3$$

$$= V_A(y_1 + y_2 + y_3) - V_B y_2 - V_o y_3$$

Using eq ② in the above

$$V_i y_1 = V_A(y_1 + y_2 + y_3) - \frac{V_o}{A_o} y_2 - V_o y_3 \quad -③$$

Apply KCL at node 'B'

$$(V_A - V_B)\,y_2 = V_B y_4$$

$$V_A y_2 = V_B y_4 + V_B y_2$$

$$V_A = \frac{V_B(y_4 + y_2)}{y_2}$$

using eq ② in above

$$V_A = \frac{V_o}{A_o} \cdot \frac{y_2 + y_4}{y_2} \quad -④$$

Substitute eq ④ in eq ③

$$V_i y_1 = \frac{V_o}{A_o}\left(\frac{y_2 + y_4}{y_2}\right)(y_1 + y_2 + y_3) - V_o y_3 - \frac{V_o}{A_o} y_2$$

$$= \frac{V_o A_o (y_2 + y_4)(y_1 + y_2 + y_3) - A_o^2 y_2 V_o y_3 - A_o y_2^2 V_o}{A_o^2 y_2}$$

$$V_i y_1 = V_o\left(\frac{A_o(y_2 + y_4)(y_1 + y_2 + y_3) - A_o^2 y_2 y_3 - A_o y_2^2}{A_o^2 y_2}\right)$$

$$\frac{V_o}{V_i} = \frac{A_o^2 y_1 y_2}{A_o(y_2 + y_4)(y_1 + y_2 + y_3) - A_o^2 y_2 y_3 - A_o y_2^2}$$

$$= \frac{A_0^2 y_1 y_2}{A_0[(y_2+y_4)(y_1+y_2+y_3) - A_0 y_2 y_3 - y_2^2]}$$

$$= \frac{A_0 y_1 y_2}{y_1y_2 + y_2^2 + y_2y_3 + y_1y_4 + y_2y_4 + y_3y_4 - A_0y_2y_3 - y_2^2}$$

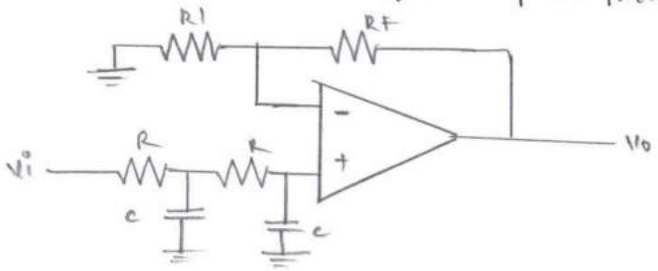
$$\frac{V_o}{V_i} = \frac{A_0 y_1 y_2}{y_1y_2 + y_2y_3 + y_1y_4 + y_2y_4 + y_3y_4 - A_0y_2y_3}$$

$$H(s) = \frac{A_0 y_1 y_2}{y_1y_2 + y_4(y_1+y_2+y_3) + y_2y_3 - A_0y_2y_3}$$

$$H(s) = \frac{A_0 y_1 y_2}{y_1y_2 + y_4(y_1+y_2+y_3) + (1-A_0)y_2y_3}$$

General expression for 2nd order filter.

2nd order butterworth low pass filter:



$$H(s) = \frac{A_0 y_1 y_2}{y_1y_2 + y_4(y_1+y_2+y_3) + (1-A_0)y_2y_3}$$

Substitute $y_1 = y_2 = \frac{1}{R}$ & $y_3 = y_4 = sc$

$$H(s) = \frac{A_0\left(\frac{1}{R^2}\right)}{\frac{1}{R^2} + sc\left(\frac{1}{R} + \frac{1}{R} + sc\right) + (1-A_0)\frac{sc}{R}}$$

$$= \frac{\frac{A_0}{R^2}}{\frac{1+R^2sC\left(\frac{2}{R}+sC\right)+(1-A_0)R^2\frac{sC}{R}}{R^2}}$$

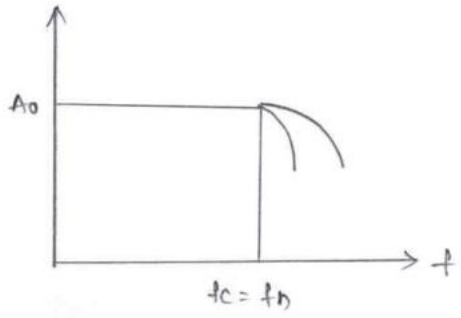
$$= \frac{A_0}{1+2sRC+s^2R^2C^2+(1-A_0)sRC}$$

$$= \frac{A_0}{1+2RC+s^2R^2C^2+sRC-A_0sRC}$$

$$= \frac{A_0}{s^2R^2C^2+3sRC-A_0sRC+1}$$

$$\boxed{H(s) = \frac{A_0}{s^2R^2C^2+(3-A_0)sRC+1}}$$

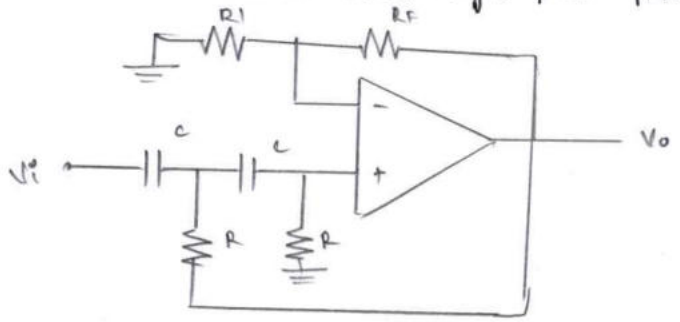
Frequency response



If $s = 0$ $H(s) = A_0$

If $s = \infty$ $H(s) = 0$

2nd order butterworth high pass filter



$$H(s) = \frac{A_0 y_1 y_2}{y_1y_2+y_4(y_1+y_2+y_3)+(1-A_0)y_2y_3)}$$

Substitute $y_1 = y_2 = sC$ & $y_3 = y_4 = \frac{1}{R}$

$$H(s) = \frac{A_0 s^2 C^2}{s^2C^2 + \frac{1}{R}(sC + sC + \frac{1}{R}) + (1 - A_0)\frac{sC}{R}}$$

$$= \frac{A_0 s^2 C^2}{s^2C^2 + \frac{2sC}{R} + \frac{1}{R^2} + \frac{sC}{R} - \frac{A_0 sC}{R}}$$

$$= \frac{A_0 s^2 C^2 R^2}{s^2C^2R^2 + 2sCR + 1 + sCR - A_0 sCR}$$

$$\boxed{H(s) = \frac{A_0 s^2 C^2 R^2}{s^2C^2R^2 + (3 - A_0)sCR + 1}}$$

Let $\omega_l = \frac{1}{RC}$, $RC = \frac{1}{\omega_l}$

$$H(s) = \frac{\frac{A_0 s^2}{(\omega_l)^2}}{\frac{s^2}{\omega_l^2} + (3 - A_0)\frac{s}{\omega_l} + 1} = \frac{\frac{A_0 s^2}{(\omega_l)^2}}{\frac{s^2 + (3 - A_0)s\omega_l + (\omega_l)^2}{(\omega_l)^2}}$$

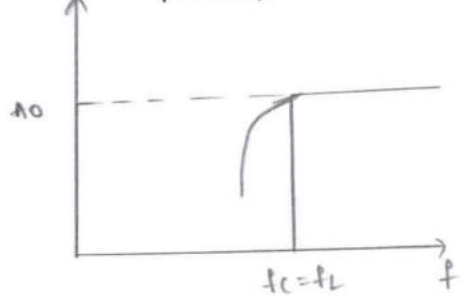
$$H(s) = \frac{A_0 s^2}{s^2 + (3 - A_0)s\omega_l + (\omega_l)^2}$$

Divide Nr & Dr with s^2

$$= \frac{A_0}{1 + (3 - A_0)\frac{\omega_l}{s} + \frac{(\omega_l)^2}{s^2}} = \frac{A_0}{\frac{(\omega_l)^2}{s^2} + (3 - A_0)\frac{\omega_l}{s} + 1}$$

$$\boxed{H(j\omega) = \frac{A_0}{\left(\frac{\omega_l}{j\omega}\right)^2 + (3 - A_0)\frac{\omega_l}{j\omega} + 1}}$$

Frequency response:



If $\omega = 0$ $H(j\omega) = 0$

If $\omega = \infty$ $H(j\omega) = A_0$

UNIT-3 : TIMER AND CONVERTERS

Timer

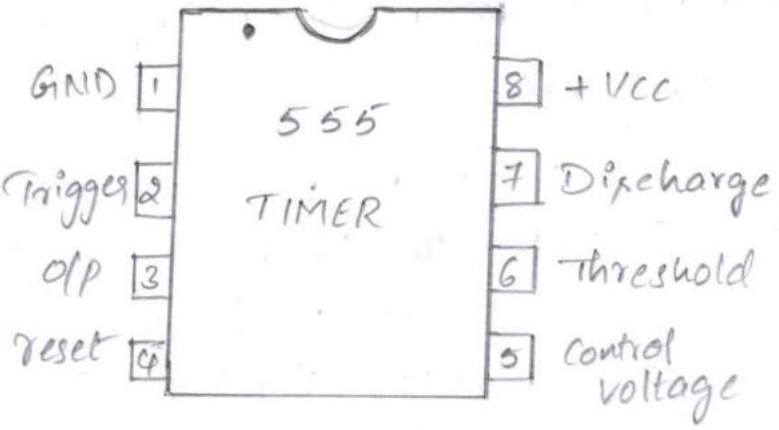
Introduction to IC555 timer

→ 555 timer is a timing circuit that can produce accurate and high stable time delays (or) Oscillations

→ 555 timer is available in 8 pin DIP & 14 Pin DIP packages

→ It can be used with supply voltages range in b/w +5V to +18V

→ The below fig. shows pin diagram of 8 pin DIP package



Features

* It can be used with supply voltages over a range in b/w +5V to +18V
* It is easy to use
* It can drive load upto 200mA
* It is compatable with TTL (Transistor transistor Logic) & CMOS (complimentary metal oxide semiconductor)

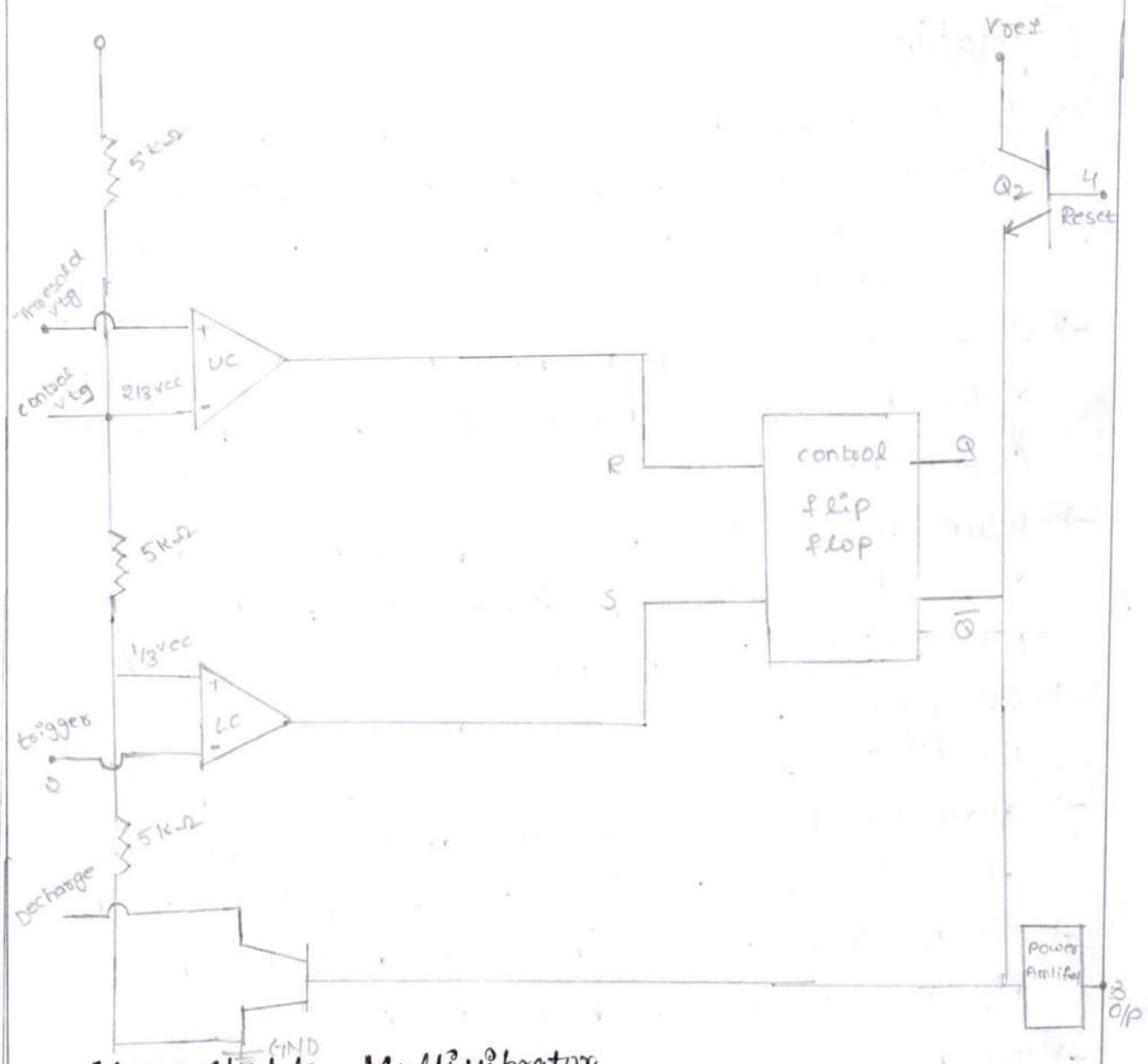
* It is used in various applications such as square wave generator, ramp & pulse wave generator, astable and monostable multivibrators

Functional Diagram

- It consists of 2 comparators namely upper comparator and lower comparator that can drive set (S) & reset (R) terminals of a flipflop
- These flipflops can control the ON & OFF cycles of the discharge transistor Q_1
- It has 3, 5 kΩ resistors which acts as potential divides, providing biasing voltages of 2/3 V_{cc} to the upper comparator & 1/3 V_{cc} to the lower comparator where V_{cc} = Supply voltages
- These voltages are called as reference voltages. These are required to control the timing
- The timing can be controlled by externally applying voltage to the control voltage terminal
- If no such control voltage is required then the control voltage terminal can be bypassed by a capacitor to ground
- Typically the capacitor value is choosen of about 0.1 μF

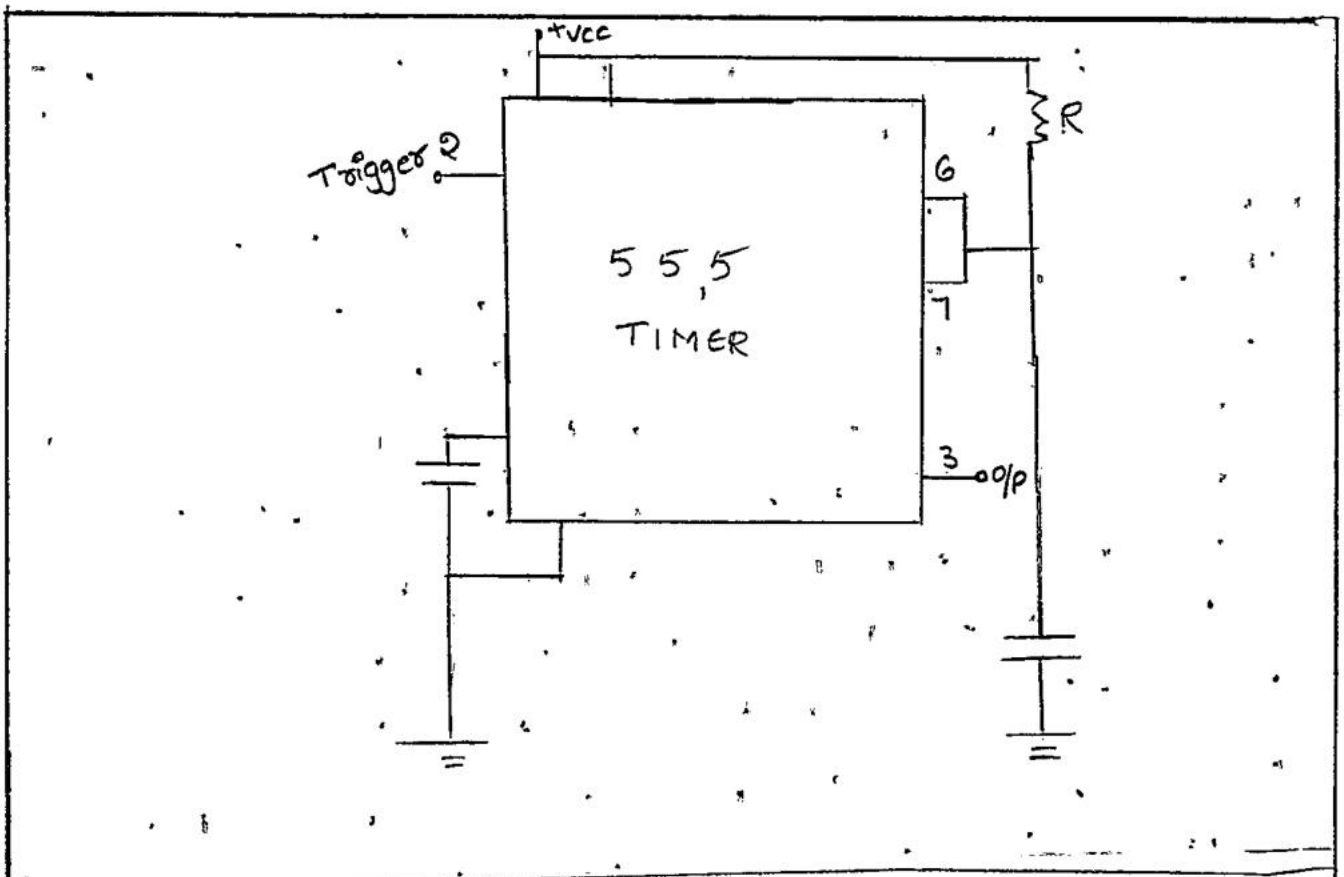
Operation

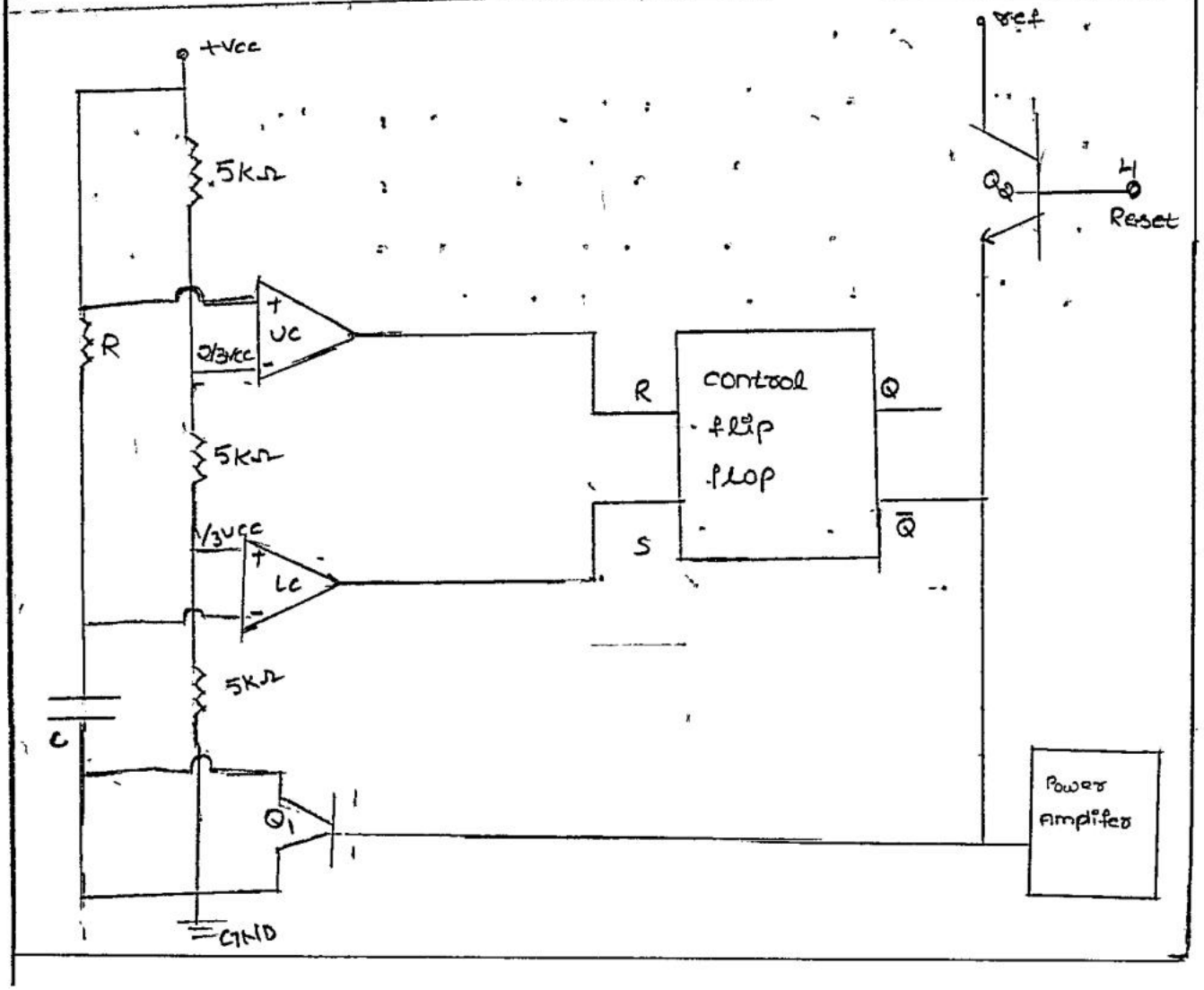
- In the stand by state (stable state), the o/p $\bar{Q}$ of the control flipflop is high ($\bar{Q}=1$; $Q=0$). This makes o/p low because of power amplifier can be acts as a inverter
- A -ve triggering pulse passes through $\frac{Vcc}{3}$, the o/p of the lower comparator goes high & sets the flipflop ($Q=1$; $\bar{Q}=0$)
- When the threshold voltage at pin 6 passes through 2/3 Vcc the o/p of upper comparator goes high & resets the flipflop ($Q=0$; $\bar{Q}=1$)
- A seperate reset terminal is produced to reset of the flipflop externally
- Normally the reset terminal is not used. if we need it should be connected to +ve supply voltage Vcc
- The transistor Q_2 acts as buffer to isolate the reset i/p from the flipflop & the transistor Q_1
- The transistor Q_1 is driven by an internal reference voltage Vref obtained from supply voltage Vcc
- If $\bar{Q}$ is high ; the transistor Q_1 is ON due to this it becomes s/c in b/w discharge pin to ground. Similarly $\bar{Q}$ is low, the transistor Q_1 is OFF & it becomes open circuit in b/w discharge pin to ground.



Monostable Multivibrator

Monostable multivibrator is a circuit which generates the non-sinusoidal signals. It has one stable state and one quas stable state. The below fig. shows the monostable multivibrator by using 555 times.


+Vcc
R
Trigger 2
6
555
TIMER
7
3
o/p


+Vcc
5KΩ
R
+
Uc
-
2/3Vcc
5KΩ
1/3Vcc
+
Lc
-
5KΩ
C
Q1
GND
Ref
Q
4
Reset
R
control
flip
flop
Q
S
$\bar{Q}$
Power
Amplifier

The above fig. shows functional block diagram of monostable multivibrator.

1) In the stand by state (stable state) $Q=0$; $\bar{Q}=1$ so o/p is low. Under this condition transistor is ON i.e; it becomes short circuit through capacitors 'c' to the ground.

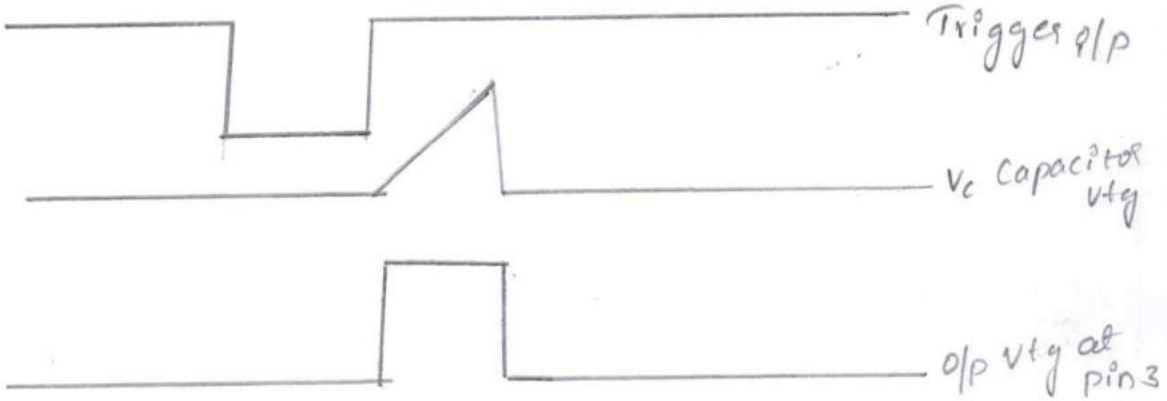
2) Now the triggering passes through $V_{cc}/3$ at 2nd pin. due to this lower comparator o/p is high. so $Q=1$, $\bar{Q}=0$ thus makes transistor Q_1 OFF & it becomes a open circuit across the capacitor so o/p is high

3) Now. the capacitor takes charging by V_{cc}

4) After a time period T, the capacitor voltage is just greater than 2/3 V_{cc} and upper comparator o/p is high so $Q=0$; $\bar{Q}=1$

5) Under the condition o/p is low & transistor Q_1 goes on there by discharging capacitor 'c' rapidly to ground

6) The corresponding o/p waveforms of monostable multi-vibrator is shown in fig.



Analysis of time Constant

The capacitor voltage across the capacitor is given by

$$V_c = V_{cc}(1 - e^{-t/RC}) \quad \text{——(1)}$$

At $t = T$, the capacitor charges by $V_c = 2/3\ V_{cc}$ —(2)

Sub Eq (2) in Eq^n (1)

$$2/3\ V_{cc} = V_{cc} - V_{cc}\, e^{-t/RC}$$

$$2/3\ V_{cc} + V_{cc}\, e^{-t/RC} = V_{cc}$$

$$e^{-t/RC} = \frac{V_{cc} - 2/3\ V_{cc}}{V_{cc}}$$

Apply log on Both sides

$$\ln(a/b) = -\ln[b/a]$$

$$\ln\left[e^{-T/RC}\right] = \ln\left[\frac{V_{cc} - 2/3\ V_{cc}}{V_{cc}}\right]$$

$$-\frac{T}{RC} = -\ln\left[\frac{V_{cc}}{V_{cc} - 2/3 V_{cc}}\right]$$

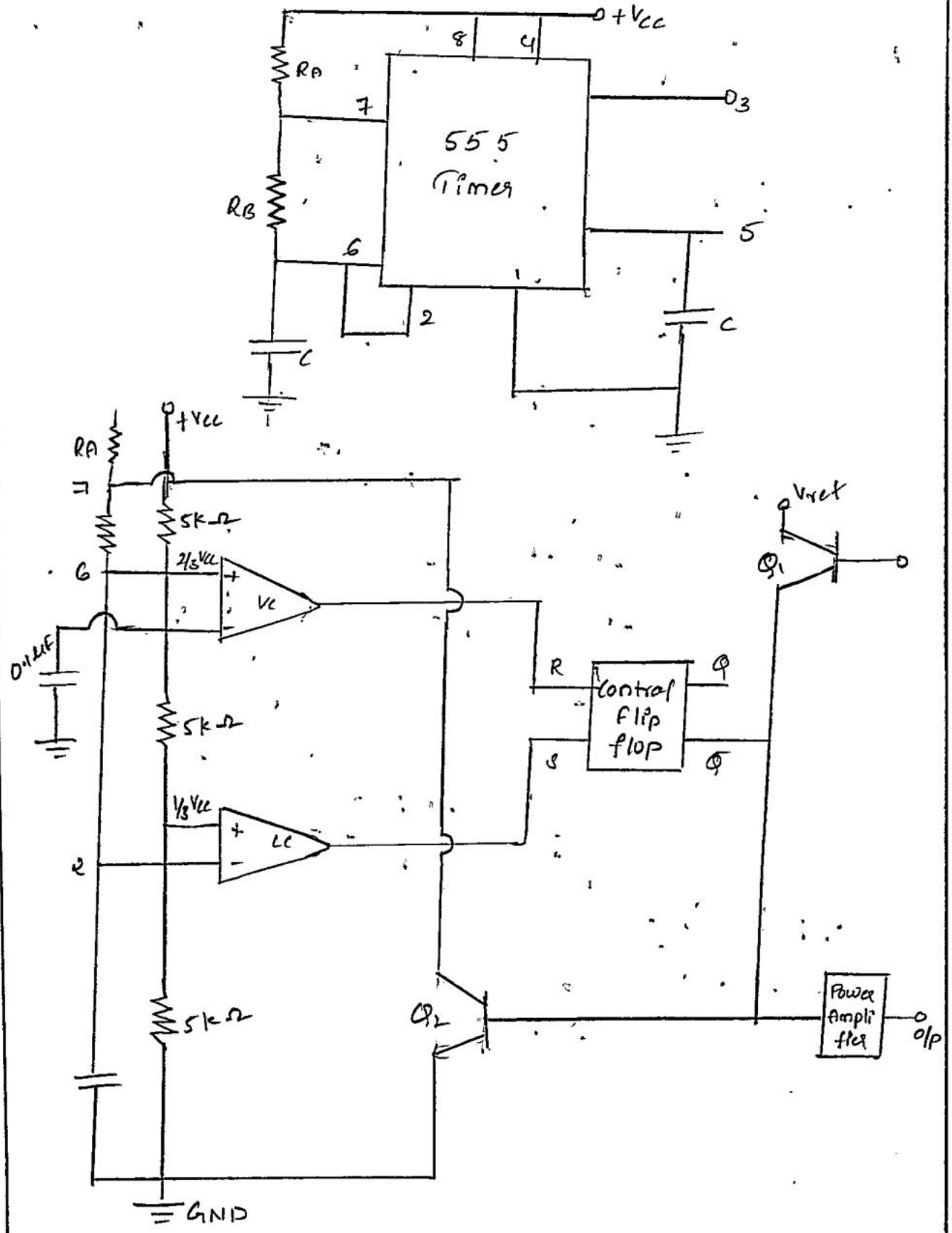
$$T = \ln RC[3]$$

$$\therefore T = 1.1\,RC$$

Applications

* Pulse width generator
* Water level control

Astable Multivibrator



Operation

1) Astable multivibrator has no stable states. It has 2 quasi stable states

2) The astable multivibrator circuit by using 555 timer is shown in above fig.

3) Comparing with monostable multivibrator, the timing resistor is now split into 2 sections i.e, R_A & R_B

4) The charging voltage reaches the 1/3 V_{cc} voltage then lower comparator goes high. Due to this $R=0$; $S=1$; $\bar{Q}=0$; $Q=1$ and therefore o/p is high

5) The discharging transistor Q_1 is connected in b/w R_A & R_B

6) When supply voltage is connected, the external capacitor gets charging through R_A & R_B resistors

7) Similarly when charging voltage reaches 2/3 V_{cc} then upper comparator o/p goes high. Due to this $R=1$; $S=0$; $\bar{Q}=1$; $Q=0$ and the o/p becomes low

8) When $\bar{Q}=1$, the discharging transistor Q_2 is ON & it makes short circuited across the capacitor

9) So the capacitor gets discharging through R_B resistor towards the ground. The capacitor discharging voltage reaches 1/3 V_{cc} & again lower comparator o/p goes high

10) The corresponding waveforms of astable multivibrator is shown in fig

Analysis of time constant

$$V_c = V_{cc}(1 - e^{-t/RC}) \quad \text{---} (1)$$

at $t = t_1$, $V_c = 1/3\, V_{cc}$

$$1/3\, V_{cc} = V_{cc} - V_{cc} e^{-t_1/RC}$$

$$V_{cc} e^{-t_1/RC} = V_{cc} - 1/3\, V_{cc}$$

$$e^{-t_1/RC} = \frac{V_{cc} - 1/3\, V_{cc}}{V_{cc}}$$

Taking log on B.S

$$\frac{-t_1}{RC} = \log\left[\frac{V_{cc} - 1/3\, V_{cc}}{V_{cc}}\right]$$

$$t_1 = RC \ln\left(\frac{1}{1 - 1/3}\right)$$

$$t_1 = RC \ln(1.5)$$

$$\therefore t_1 = 0.405\, RC$$

→ When the capacitor charges from $1/3\, V_{cc}$ to $2/3\, V_{cc}$

at $t = t_2$; $V_{cc} = 2/3\, V_{cc}$

$$2/3\, V_{cc} = V_{cc} - V_{cc} e^{-t_2/RC}$$

$$V_{cc} e^{-t_2/RC} = V_{cc} - 2/3\, V_{cc}$$

$$e^{-t_2/RC} = \frac{V_{cc} - 2/3\, V_{cc}}{V_{cc}}$$

Taking log on b.s

$$-t_2/RC = \ln\left[\frac{V_{CC} - 2/3\,V_{CC}}{V_{CC}}\right]$$

$$t_2 = \ln RC\left[\frac{V_{CC}}{V_{CC} - 2/3\,V_{CC}}\right]$$

$$t_2 = RC\ln(3)$$

$$\therefore t_2 = 1.1RC$$

$$T_C = t_2 - t_1$$

$$= 1.1 - 0.405$$

$$= 0.695RC$$

$$\therefore T_C = 0.695(R_A + R_B)C$$

→ The capacitor takes discharging from $2/3\,V_{CC}$ to $1/3\,V_{CC}$

$$1/3\,V_{CC} = 2/3\,V_{CC}\,e^{-t/RC}$$

$$e^{-t/RC} = \frac{1/3\,V_{CC}}{2/3\,V_{CC}}$$

$$e^{-t/RC} = 1/2$$

$$-t/RC = \ln(1/2)$$

$$t/RC = \ln(2)$$

$$t = RC\ln(2)$$

$$\therefore T_d = 0.69\,R_BC$$

=> The total time constant $T = T_C + T_D$

$$T = 0.69(R_A + R_B)C + 0.69 R_B C$$

$$= 0.69 R_A C + 0.69 R_B C + 0.69 R_B C$$

$$\therefore T = 0.69(R_A C + 2R_B C)$$

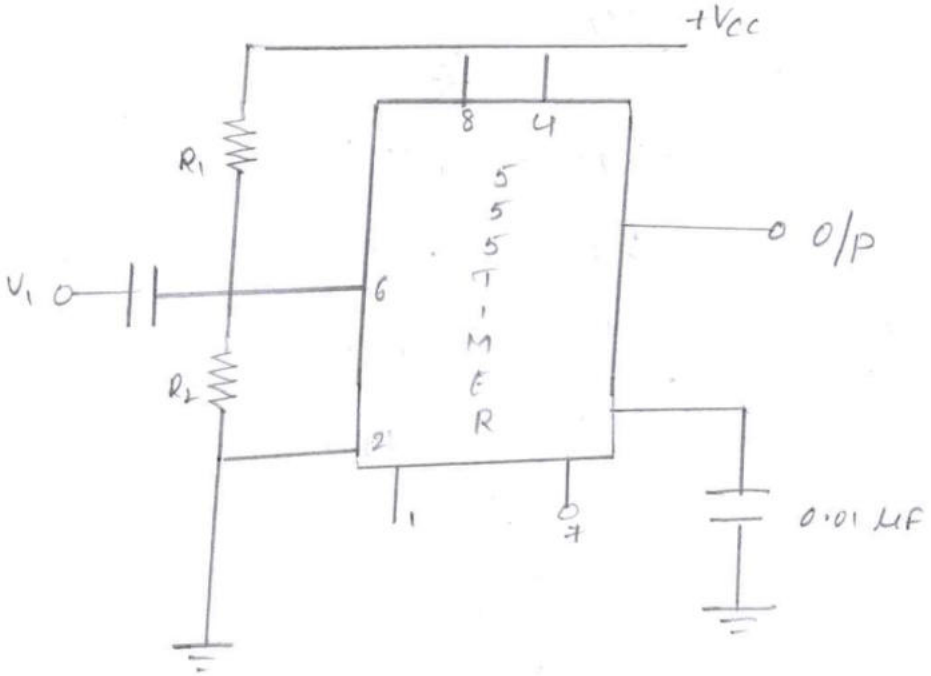
$$f = 1/T$$

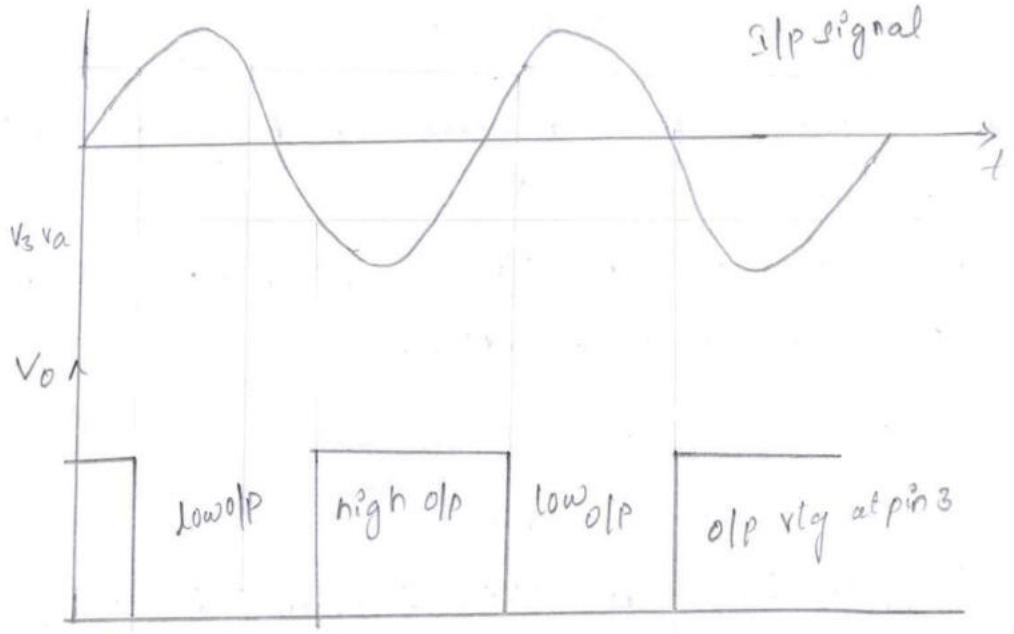
$$= \frac{1}{0.69(R_A + 2R_B)C}$$

$$\therefore f = \frac{1.449}{(R_A + 2R_B)C}$$

Applications

1) Frequency shift key (FSK)
2) Pulse Position Modulator
Schmitt Trigger





→ Here 2 internal comparators are connected together an externally based through R_1 & R_2 registers

→ Since Upper comparators will be ON (or) o/p is high when the given i/p signal reaches the $2/3 V_{CC}$

→ Similarly lower comparator o/p is high when the given i/p signal reaches the $1/3 V_{CC}$

→ Due to that the o/p of the circuit is changing from one state to another state i.e, when Vc is high, o/p is low when Vc is high, o/p is high

(R=0 ; S=1 ; Q=1 ; $\bar{Q}$=0)

Function

* Eliminates noise from input signals
* Converts a slowly changing input into a sharp, fast-changing output.

Transfer Characteristics

* It shows the hysteresis loop instead of a single threshold.
* This prevents multiple unwanted switching due to small noise fluctuations.

Circuit Implementation

Can built using:

- Operational amplifier (OP-amp) in comparator mode with positive feedback
- Transistors (BJT or MOSFET)
- Logic gates (like TTL or CMOS inverters with feedback)

Applications

* Removing noise in digital signals
* Square wave generation from sine or triangular signals
* Pulse shaping
* Debouncing switches
* Used in ADCs, waveform generators,

D to A and A to D converters:

Introduction:

1) A/D converter (Analog - to - Digital)

Definition

A A/D converter changes a continuous - time analog signal into a discrete - time digital signal

- **Need**

Digital systems cannot directly understand analog signals from sensors, so A/D conversion is necessary

- **Process**

a) Sampling → Take values of the analog signal at regular time intervals

b) Quantization → Approximate each sampled value into a finite set of levels

c) Encoding → Represent the quantized levels as binary code.

- **Types**

* Flash ADC
* Successive Approximation Register
* Dual - slope ADC
* Sigma - Delta ADC

D/A converter (Digital-to-Analog converter)

→ Definition

A D/A converter changes a digital signal back to a continuous analog signal

- Need

Many real-world devices need analog signals. Computers generate digital data, so converting back to analog is essential

- Process

a) Binary input is given
b) A weighted sum of voltages / currents is generated
c) Output is a staircase-like signal, which is often smoothed using filters

- Types

* Weighted ~~Reg~~ Resistor DAC
* R-2R Ladder DAC
* Sigma-Delta DAC

Basics DAC Techniques

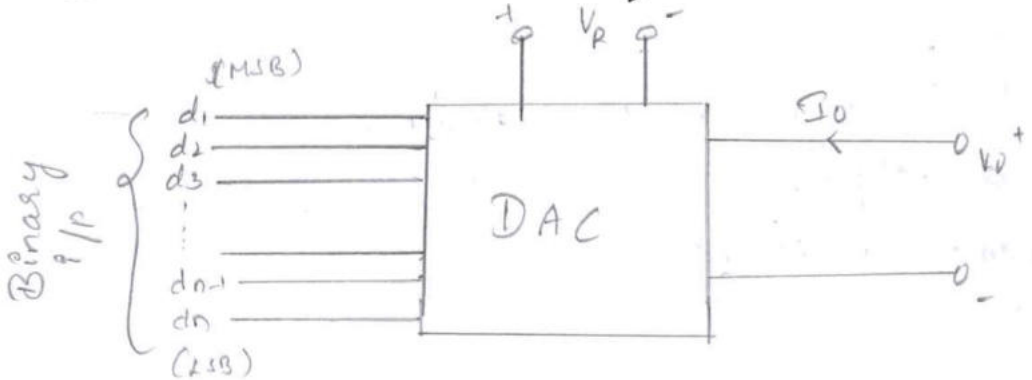


fig: Schematic of DAC

1) The i/p is an n-bit binary word D and is combined with a reference voltage V_R to give an analog o/p signal

2) The o/p of a DAC can be either of a voltage (or) current

3) for a voltage o/p DAC, the D/A convertor is mathematically described as

$$V_0 = k V_{FS}(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

where

V_0 = o/p voltage

V_{FS} = full scale o/p voltage

k = scaling factor = unity

$d_1 \cdots d_n$ = n bit binary fractional word with the decimal point located at the left

d_1 = MSB bit

d_n = LSB bit

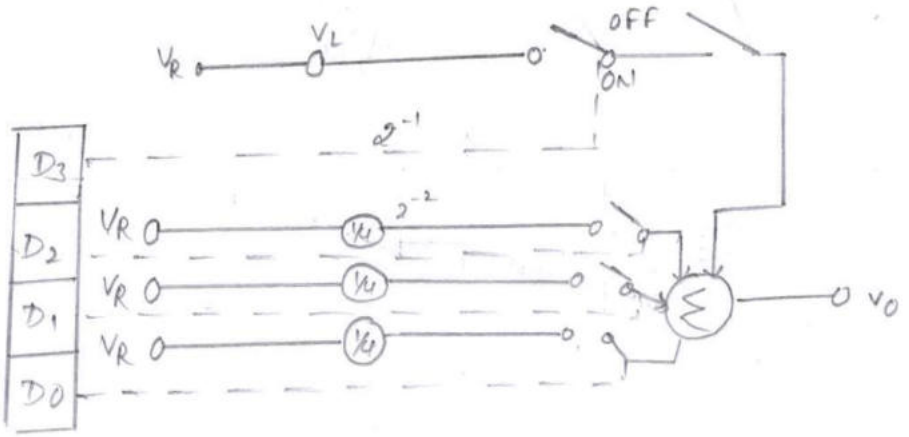


fig: Digital to Analog conversion

- Fig. shows explanation of DAC. Here V_R is a fixed reference voltage.
- The digital signal is contained in the register on the left
- Each flipflop in the register controls an analog switch as shown in the dotted lines

$$V_0 = \left[D_3 2^{-1} + D_2 2^{-1} + D_1 2^{-3} + D_0 2^{-4}\right] V_R$$

if $D_3 D_2 D_1 D_0 = 1001$

$$V_0 = 1 \times \left[\frac{V_R}{2} + 0\frac{V_R}{4} + 0\frac{V_R}{8} + 1\frac{V_R}{16}\right]$$

$$\boxed{V_0 = \frac{9V_R}{16}}$$

- There are 2 types D/A converter
  1. Weighted resistor D/A converter
  2. R-2R ladder D/A converter

1. Weighted - resistor D/A converter

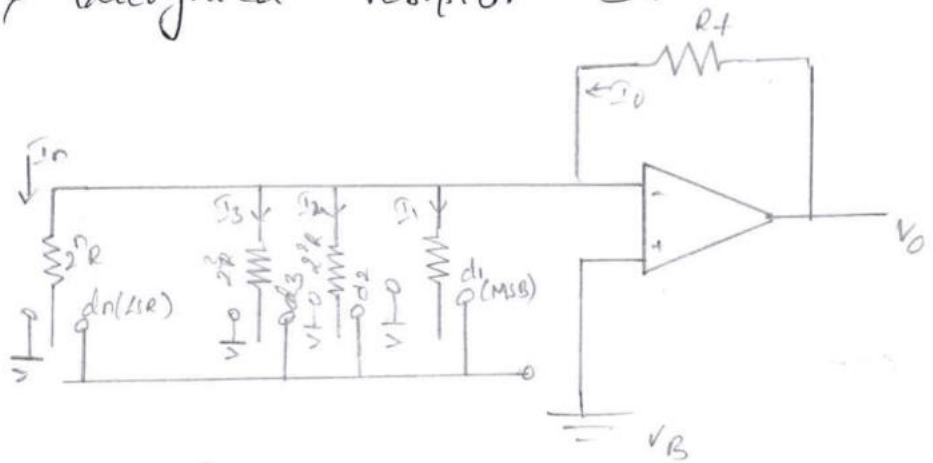


fig: A simple weighted Resistor DAC

- One of the simplest ckt uses a summing amplifier with a binary weighted resistor N/W. It has n-electronic switches $d_1, d_2 \ldots \ldots d_n$ controlled by binary i/p word.
- These switches are SPDT (Single Port Double Throw) types switch

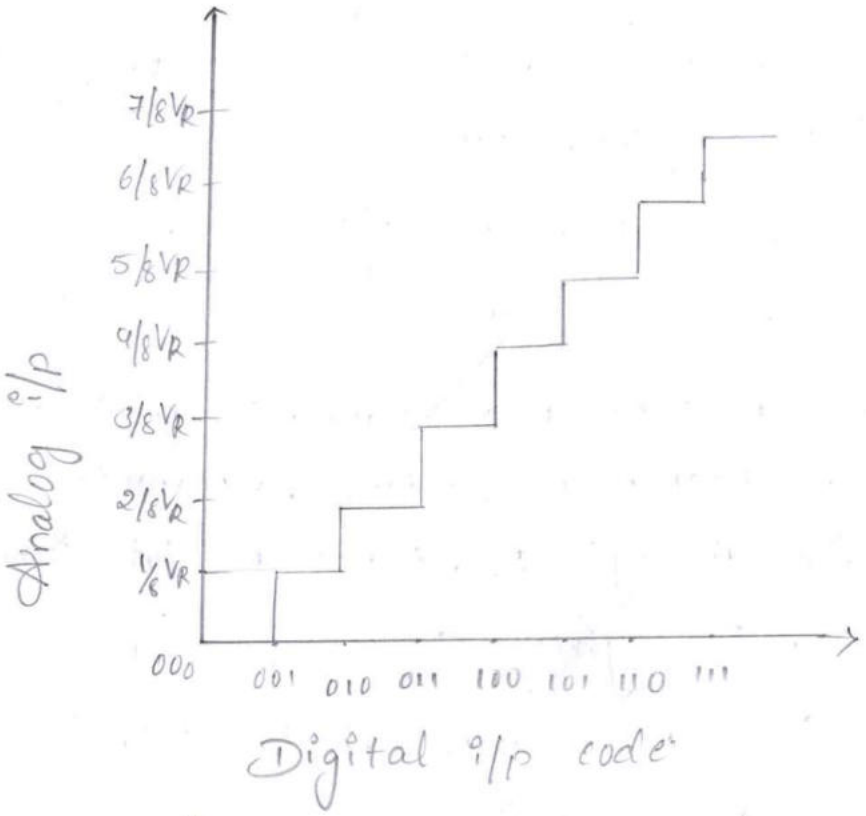


fig : Transfer char's of a 3bit DAC

- The binary weighted resistor DAC uses an op-amp to sum of 'n' binary weighted ~~resistor~~ currents derived from a reference voltage V_R via current scalling resistors $\cdot 2R, 4R, 8R \cdots 2^n R$ as shown in fig

Working

In fig. switch positions are controlled by the digital i/p's when digital i/p logic 1. it connects the corresponding resistance to the reference voltage V_R Otherwise it leaves resistor open

$$\therefore \text{for ON switch } I = \frac{-V_R}{R}$$

$$\text{for off switch } I = 0$$

Here op-amp is used as a summing amplifier. Due to high i/p impedance of op-amp, summing current will flow through R_f. Hence the total current through R_f can be given as

$$I_0 = I_1 + I_2 + I_3 + \cdots + I_n$$

The o/p voltage is the voltage across R_f and it is given as

$$\text{so } V_0 = -I_0 R_f$$

$$V_0 = -\left[I_1 + I_2 + I_3 + \cdots I_n\right] R_f$$

$$V_0 = \left[D_1 \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \frac{V_R}{8R} + \cdots D_n \frac{V_R}{2^n R} \right] V_f$$

$$= \frac{V_R}{R} R_f \left[D_1 2^{-1} + D_2 2^{-2} + \cdots + D_n 2^{-n} \right]$$

where $R_f = R$

$$\therefore V_0 = V_R \left[D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} + \cdots + D_n 2^{-n} \right]$$

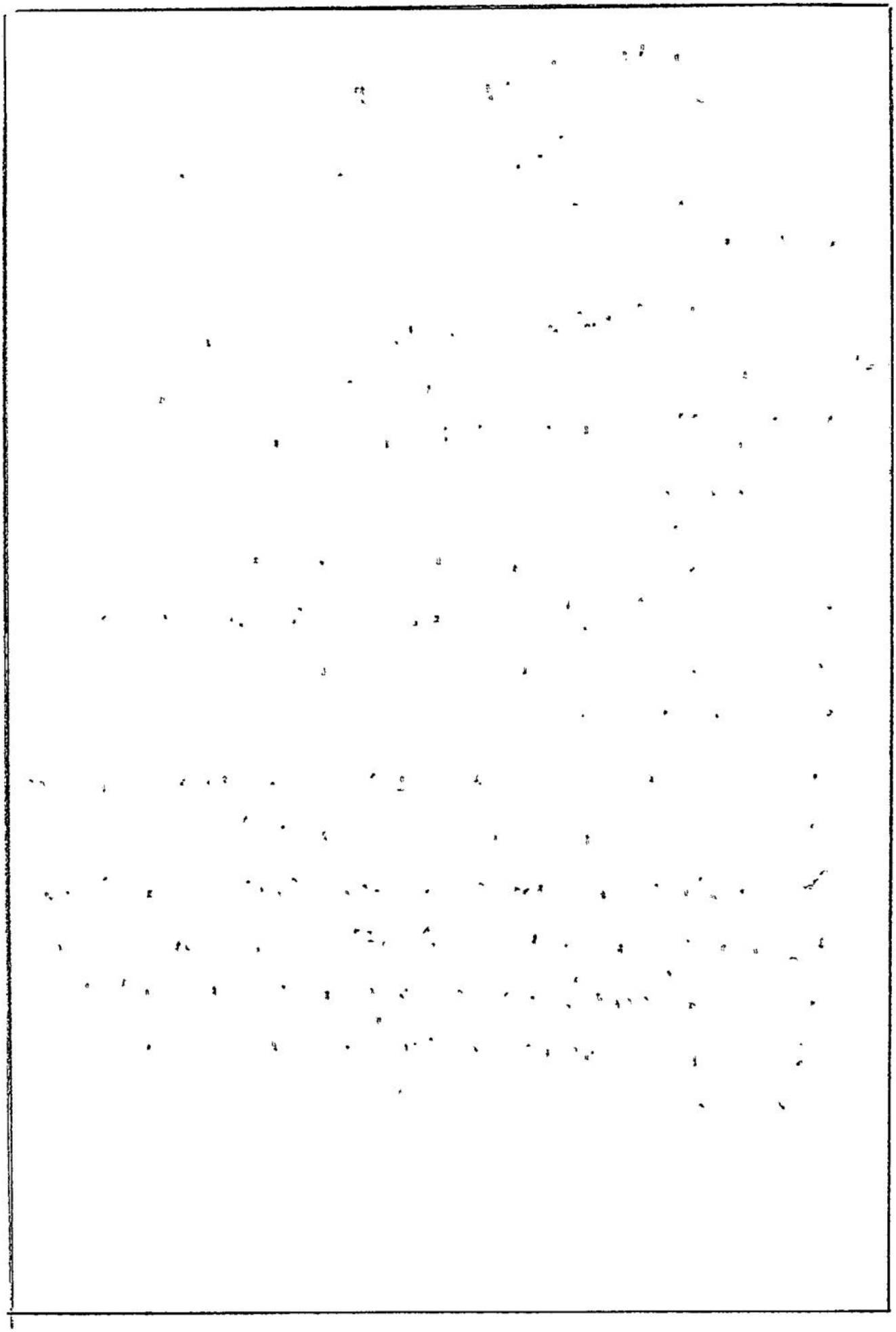
→ The above Eqn indicates that the analog o/p voltage is proportional to the i/p digital word.

Drawbacks

1) Wide range of resistor values are required for 8 bit DAC - the resistor required are 2^1R, 2^2R... and 2^8R. Therefore the largest resistor is 128 times of the smallest one

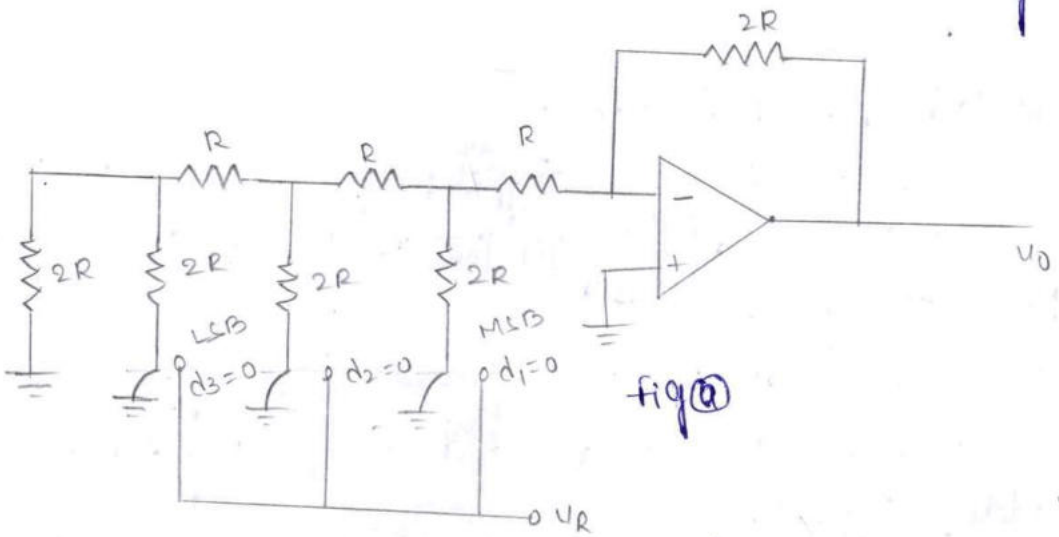
This wide range of the ~~switches~~ resistors values has restrict on both higher & lower ends

2) The infinite resistance of the switches disturbs the binary weighted relationship among the various currents, particularly in the MSB positions. where the current setting resistances are smaller



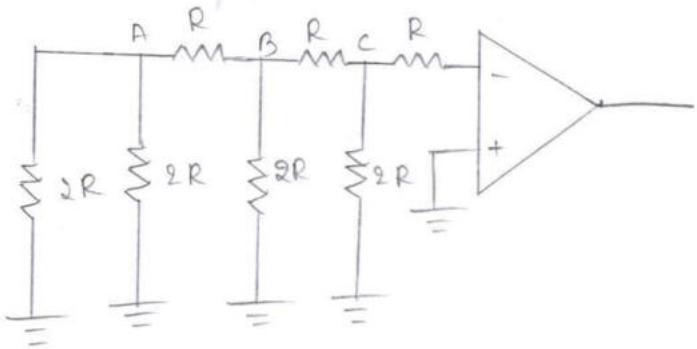
R–2R Ladder DAC:

- In this type, reference voltage is applied to one of the switch positions and other switch position is connected to ground. It is shown in below figure.
- Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only 2 values of resistors are required.
- The typical value of R ranges from 2.5kΩ to 10kΩ.
- For simplicity let us consider a 3-bit DAC, where the switch position $D_1 D_2 D_3$ corresponds to the binary word 100.

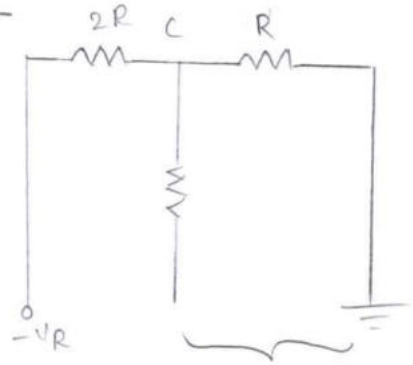


fig(a)

The equivalent circuit can be simplified as shown below. fig.



fig(b) Equivalent ckt of fig(a).



2/3R.

Equivalent ckt of fig(b)

- Then voltage of node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = \frac{-V_R}{4}$$

The o/p voltage is

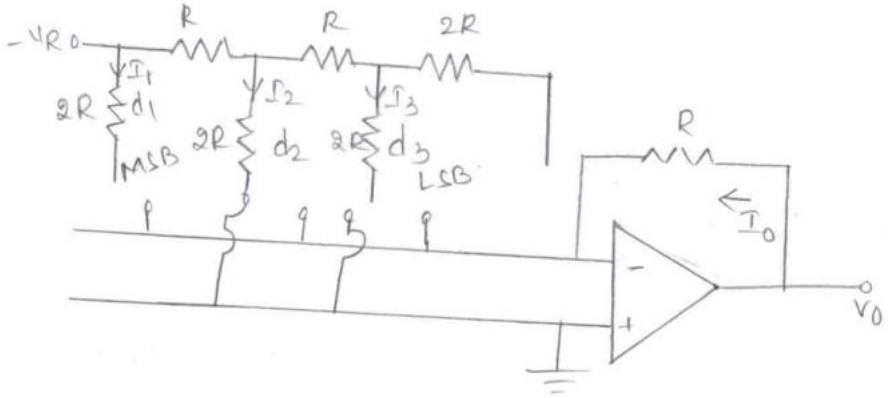
$$V_0 = \frac{-2R}{R}\left(-\frac{V_R}{4}\right)$$

$$= V_R/2$$

$$\boxed{V_0 = \frac{V_{FS}}{2}}$$

Inverted R-2R ladder:

- In weighted resistor type DAC and R-2R ladder type DAC current flowing in the resistors changes as the i/p date changes.
- More power dissipation causes heating.
- This problem can be avoided completely in inverted R-2R ladder type DAC
- R-2R ladder D/A Convertor uses only 2 resistors values.



- Here each bit of binary word Converts the Corresponding switch either to ground (or) to the inverting i/p terminal of the op-amp which is at the virtual ground.
- Since both the positions of switch are at ground potential, the current flowing through resistances is Constant and it is independent of switch position.
- These current can be given as

$$I_1 = \frac{V_R}{R}$$

$$I_2 = \frac{V_R/2}{2R}$$

$$= \frac{V_R}{4R}$$

$$I_2 = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R}$$

$$= \frac{V_R}{8R}$$

$$I_3 = I_1/4$$

W.K.T

$$V_0 = -I_0 R_f$$

$$= -R_f [I_1 + I_2 + I_3]$$

$$V_0 = -R_f \left[D_1 \cdot \frac{V_R}{2R} + D_2 \frac{V_R}{4R} + D_3 \cdot \frac{V_R}{8R} \right]$$

$$= -\frac{V_R R_f}{R} \left[D_1 2^{-1} + D_2 2^{-2} + D_3 2^{-3} \right]$$

if $R_f = R = V_0 = -V_R [D_1 2^{-1} + D_2 2^{-1} + D_3 2^{-3}]$

Let us Consider 8-bit i/p with binary 011.

Here the output voltage is given as

$$V_0 = -V_R\left(0\times 2^{-1} + 1\times 2^{-2} + 1\times 2^{-3}\right)$$

$$= -V_R\left[0 + \frac{1}{4} + \frac{1}{8}\right]$$

$$= -V_R[0.25 + 0.125]$$

$$= -V_R[0.375]$$

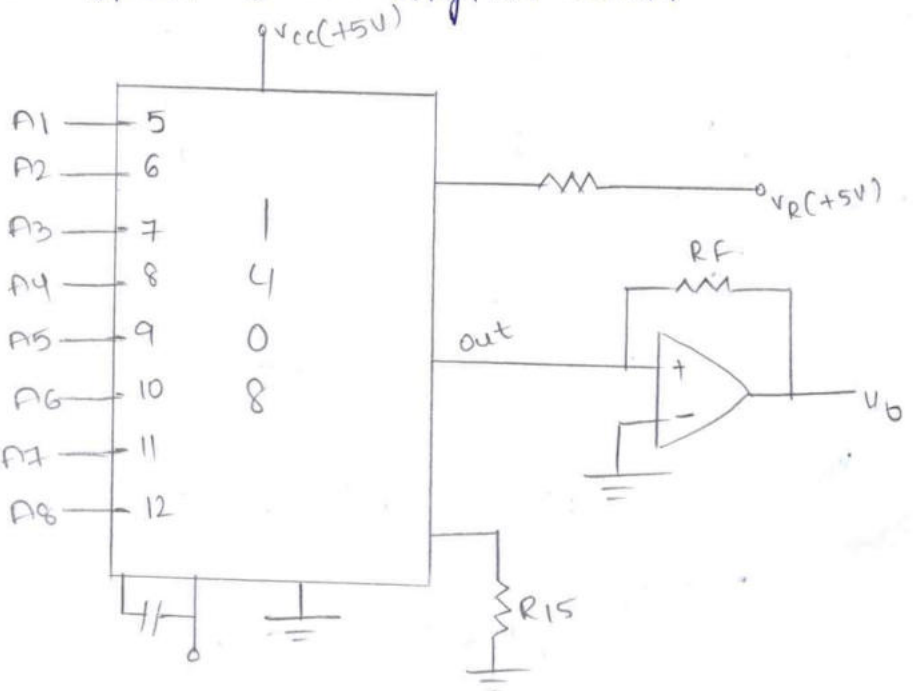
Let $V_R = 5V$

$$= -5 \times 0.375$$

$$\boxed{V_0 = -1.875V}$$

IC 1408 DAC:

- The 1408 is an 8-bit 8-2R ladder type D/A Convertor compatible with TTL and CMOS logic.
- It is designed to use where the o/p current vs linear product of an 8-bit digital word.



- The IC 1408 consists of a reference current amplifier an R/2R ladder and 8-bit high speed current switch.
- It has 8 i/p data lines as A_1 (MSB) through A_8 (LSB) which controls the positions of current switches.
- It requires 2 MA reference current for full scale i/p & 2 power supplies $V_{CC} = 5V$ and $V_{EE} = -5V$
- The voltage V_R and resistor R_{14} determines the total reference current source.

$$\text{i.e, Current } I = \frac{V_R}{R_{14}} \Longrightarrow \frac{5}{2.5K\Omega} = 2mA$$

- R_{15} is generally equal to R_{14} to match the i/p impedance of the current amplifier.
- The below fig. shown a typical 8-bit DAC 1408 compatible with TTL and CMOS logic.
- If setting time is around 300ns. (3)

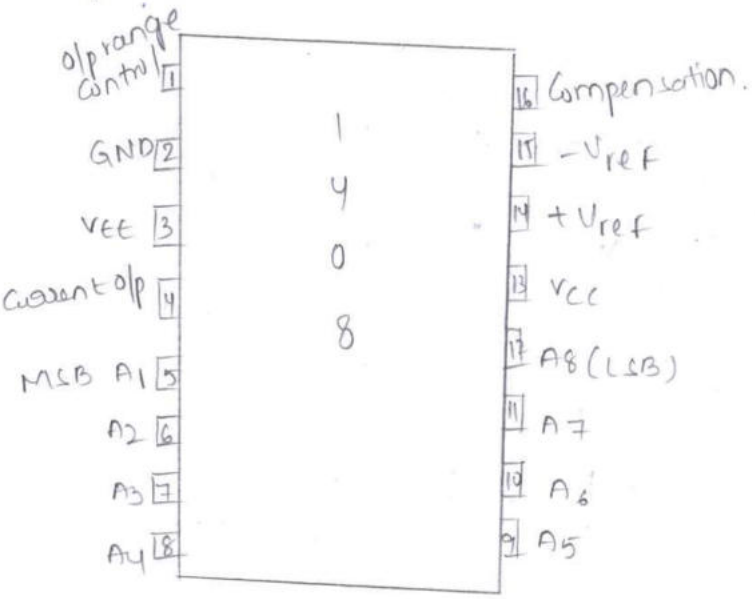


fig: Pin diagram

- It Consist of 8 input data lines A_1 (MSB) to A_8 (LSB)
- It needs 2MA reference current for full scale i/p
- The resistance R_{15} is equal to R_{14}. Hence match the i/p impedance of the reference source.

The o/p current I_o is given by

$$I_o = \frac{V_R}{R_{14}} \left[\sum_{i=1}^{n} A_i 2^{-i} \right]$$

$A_i = 0$ (or) 1

The total reference current is equal to

$$\frac{V_R}{R_{14}} = 5V / 2.5k\Omega = 2mA$$

for full scale i/p

$$I_o = \frac{5}{2.5k} \left[\sum_{i=1}^{8} A_i \times 2^{-i} \right]$$

$$= 1.992\ mA$$

The o/p voltage V_o for full scale i/p is

$$V_o = 2mA \left[\frac{255}{256} \right] \times 5 \times 10^3$$

$$= 9.91\ V$$

The o/p voltage equation

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \cdots + \frac{d_8}{256} \right]$$

- for the bipolar range from $-5V$ to $5V$ the 1408 DAC can calibrated by adding R_B b/w V_R and o/p voltage pin 4.

as indicated in the following fig

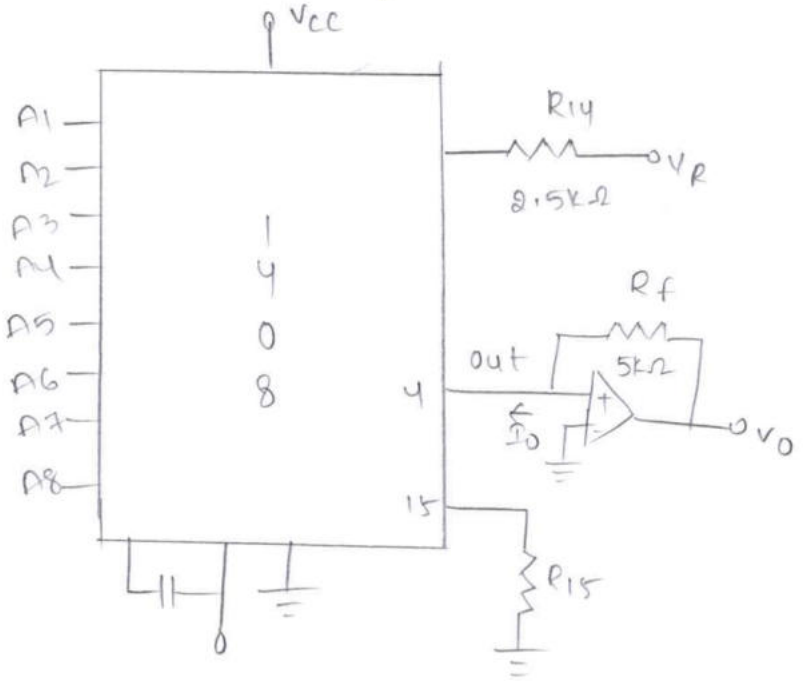
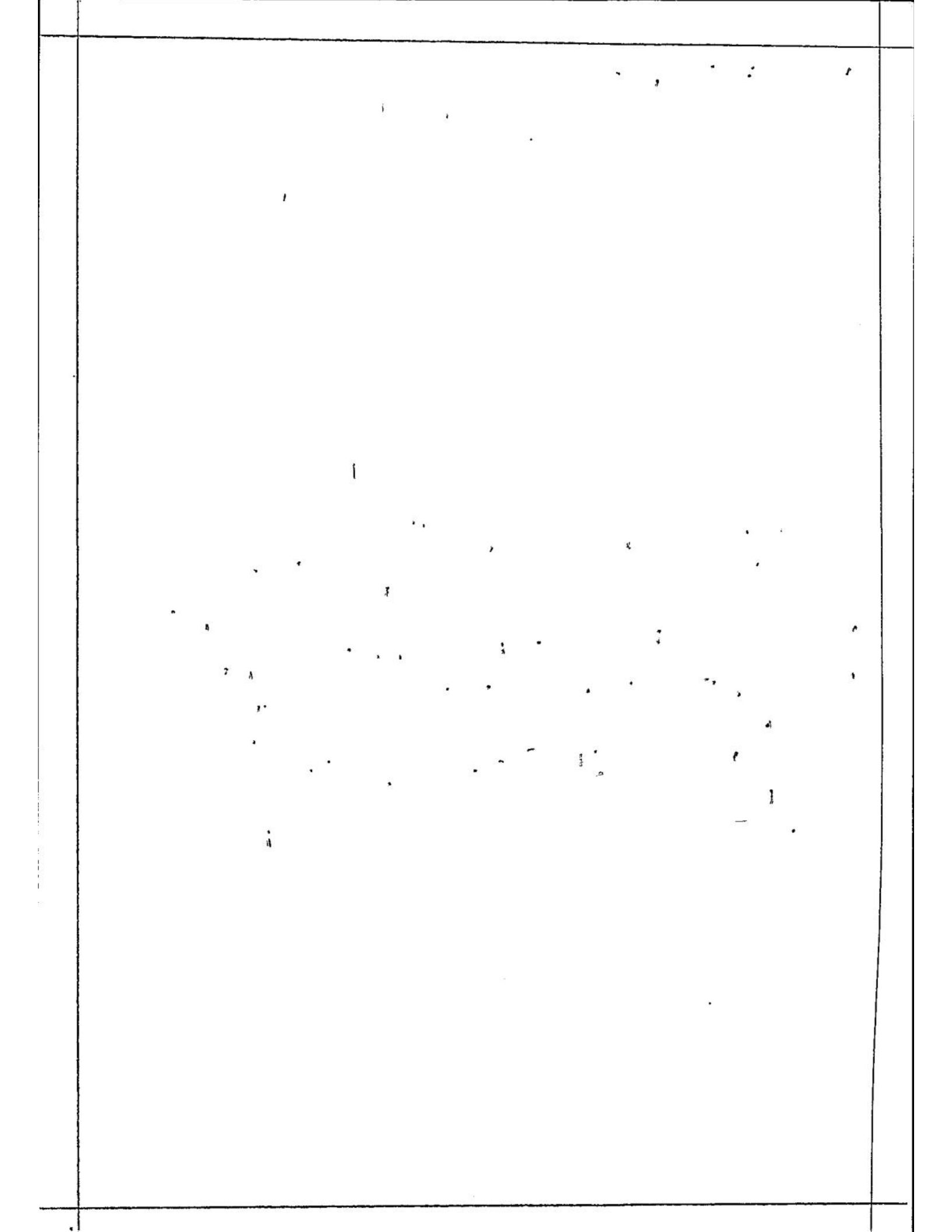


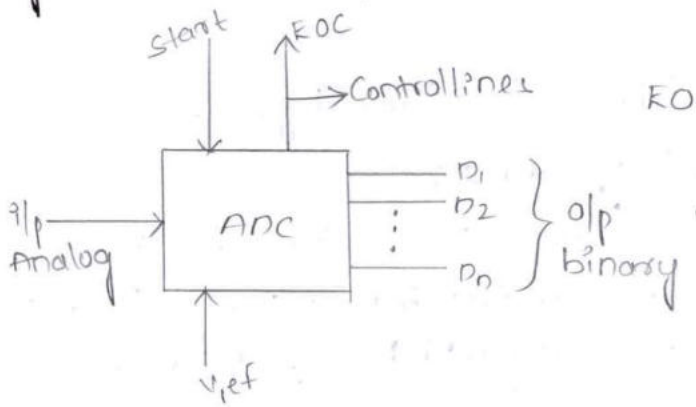
fig: 1408 D/A Converter voltage o/p voltage range in unipolar Range.

- The resistor R_B gives 1mA current to the o/p.
- The o/p current for the bipolar operation I_O' in

$$I_O = I_O - \left[\frac{V_R}{R_{14}}\right]\left[\sum_{i=1}^{8} d_i 2^{-i}\right] - \left[\frac{V_R}{R_B}\right]$$



Analog to Digital Convertors:



- The ADC, is a circuit in which analog input combines with reference voltage to give the digital o/p. The schematic representation of ADC is shown in above fig.
- ADC in a opposite version of DAC. ADC also uses the reference voltage to give an output.

The o/p equation is

$$D = d_1 2^{-1} + d_2 2^{-2} + \ldots d_n 2^{-n}$$

where d_1 = MSB, d_n = LSB

- ADC Converts of 2 control lines i.e, Start & EOC

Start: It is a input control line to tell the ADC to start the Conversion.

EOC : It is a output control line to annaunce when the Conversion is Completed.

- Depending upon the type of application ADC are designed for micro processor
- ADC are classified into 2 types:
  1. Direct type ADC.
  2. Indirect type ADC.

1. Direct Type ADC:

It Compares the given analog signal with the internally generated equivalent signal. There are classified into 3 Types:

a. Parallel Comparator Type ADC
b. Counter Type ADC
c. Successive Approximation Type ADC.

2. Integrating Type ADC:

It performs Conversion in indirect manner by first changing the analog input signal to a linear function of time & then to a digital bits. These are classified into 2 types.

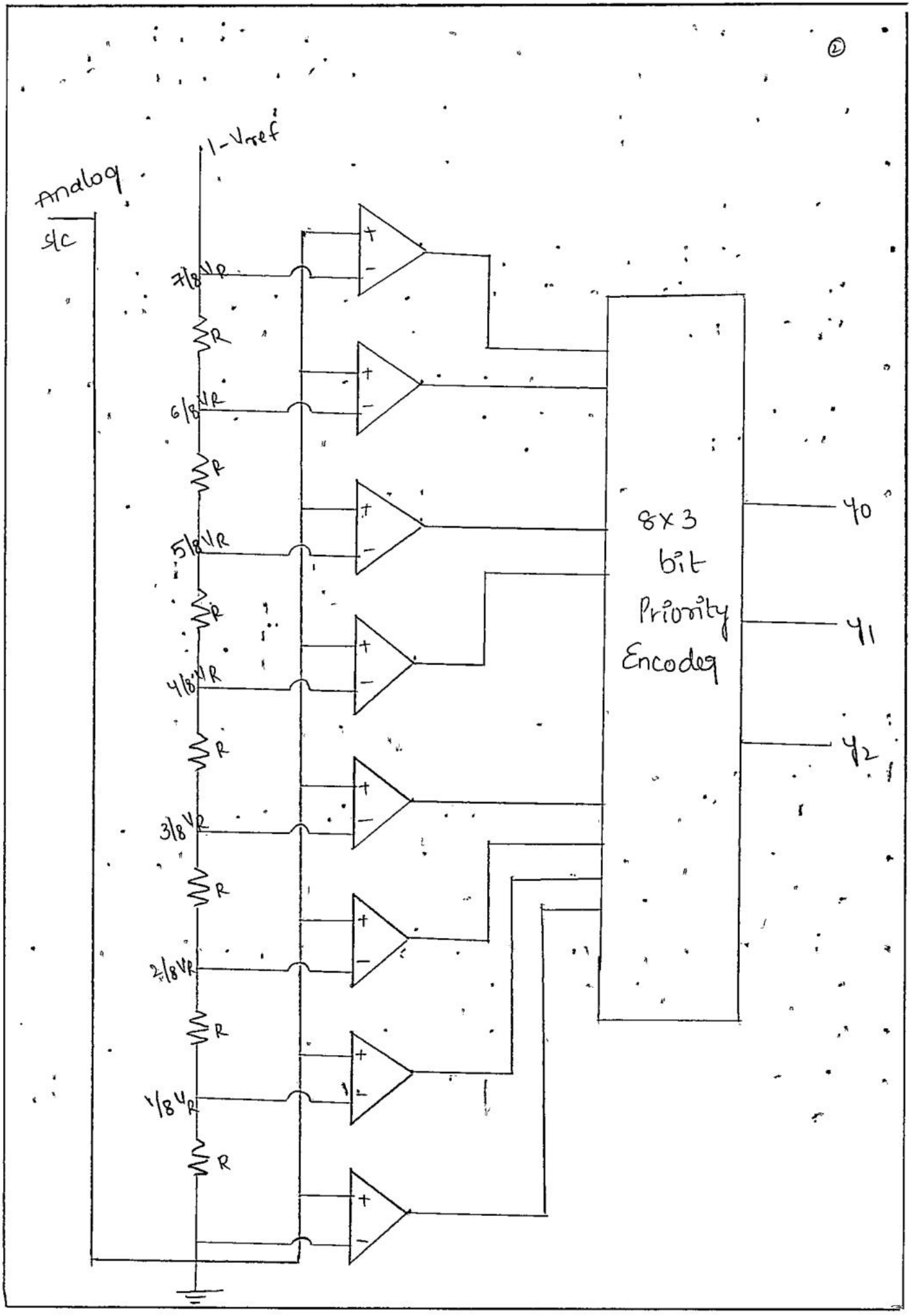
a. Dual slope type ADC
b. Charge Balance type ADC.

a. Parallel Comparator type ADC:

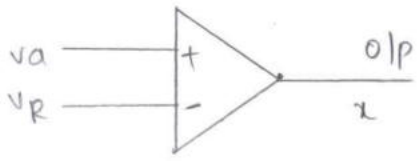
It is the simplest convertor at the same time it is fastest & most expensive Technique.

- The fig. shows the 3-bit A/D Convertor. It Consist of resistive divider network. Op-Amp comparator & priority encoder

V_o	I_0	I_1	I_2	I_3	I_4	I_5	I_6	Y_1	Y_2	Y_3
$0V_{ref}$ to $1/8 V_{ref}$	0	0	0	0	0	0	0	0	0	0
$1/8 V_{ref}$ to $2/8 V_{ref}$	1	0	0	0	0	0	0	0	0	1
$2/8 V_{ref}$ to $3/8 V_{ref}$	1	1	0	0	0	0	0	0	1	0
$3/8 V_{ref}$ to $4/8 V_{ref}$	1	1	1	0	0	0	0	0	1	1
$4/8 V_{ref}$ to $5/8 V_{ref}$	1	1	1	1	0	0	0	1	0	0
$5/8 V_{ref}$ to $6/8 V_{ref}$	1	1	1	1	1	0	0	1	0	1
$6/8 V_{ref}$ to $7/8 V_{ref}$	1	1	1	1	1	1	0	1	1	0
$7/8 V_{ref}$ to V_{ref}	1	1	1	1	1	1	1			


Analog
I/C
I-Vref
7/8VR
R
6/8VR
R
5/8VR
R
4/8VR
R
3/8VR
R
2/8VR
R
1/8VR
R
8x3
bit
Priority
Encoder
Y0
Y1
Y2

- Once input each comparator is connected to the input signal v_a & other i/p is connected to the reference signal V_R generated by the reactive divided network.
- At each node of the resistive divider equal voltage is available.
- Since all the resistive are of equal value the voltage levels available at the nodes are equally divided between V_R & GND.
- The purpose of the circuit is to compare the analog input v_a with each of the node voltages. Corresponding truth table is shown in above fig.
- The individual Comparator truth table is shown in below fig.



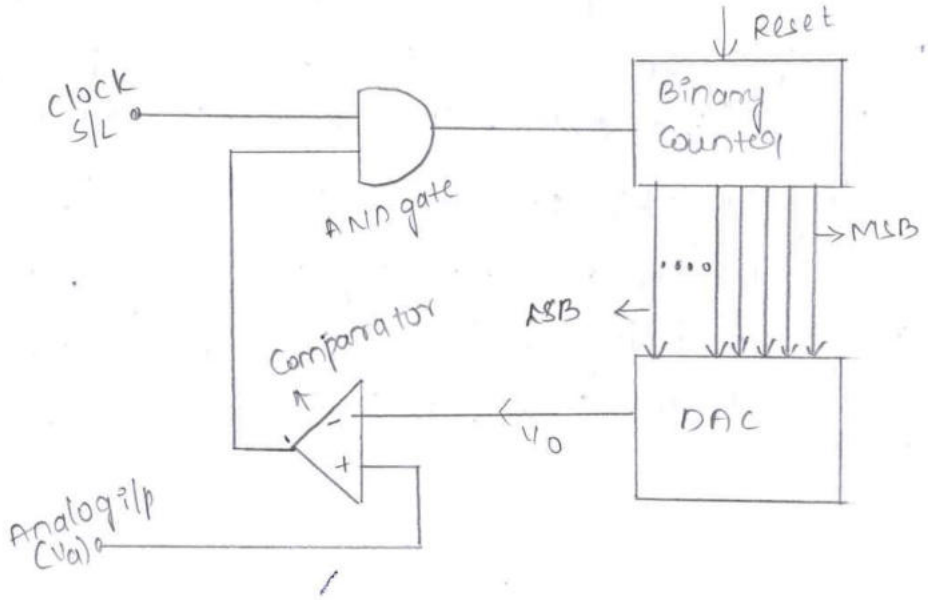
i/p's	o/p
$v_a > V_R$	x = 1
$v_a < V_R$	x = 0
$v_a = V_R$	Previous output

NOTE: It is also called as Flash Type A/D Comparator.

b. Counter Type ADC:

It is one type of analog to digital Convertor.

- Here the output of DAC is continuously Compared with the i/p analog signal.
- When the output of DAC is greater than analog input then only the output Comparator is high.
- The block diagram of Counter type ADC is shown in fig.
- It consists of a binary Counter, DAC, Comparator & AND gate.

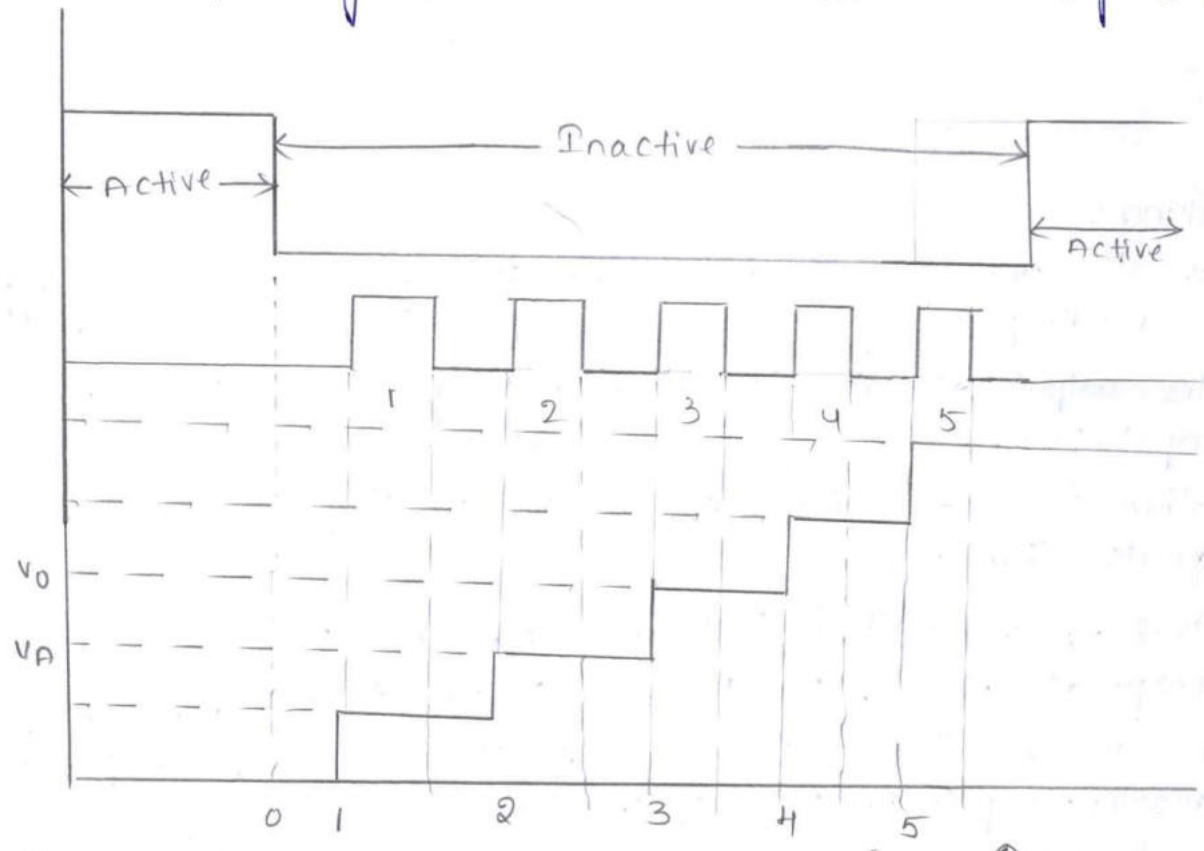


Working:

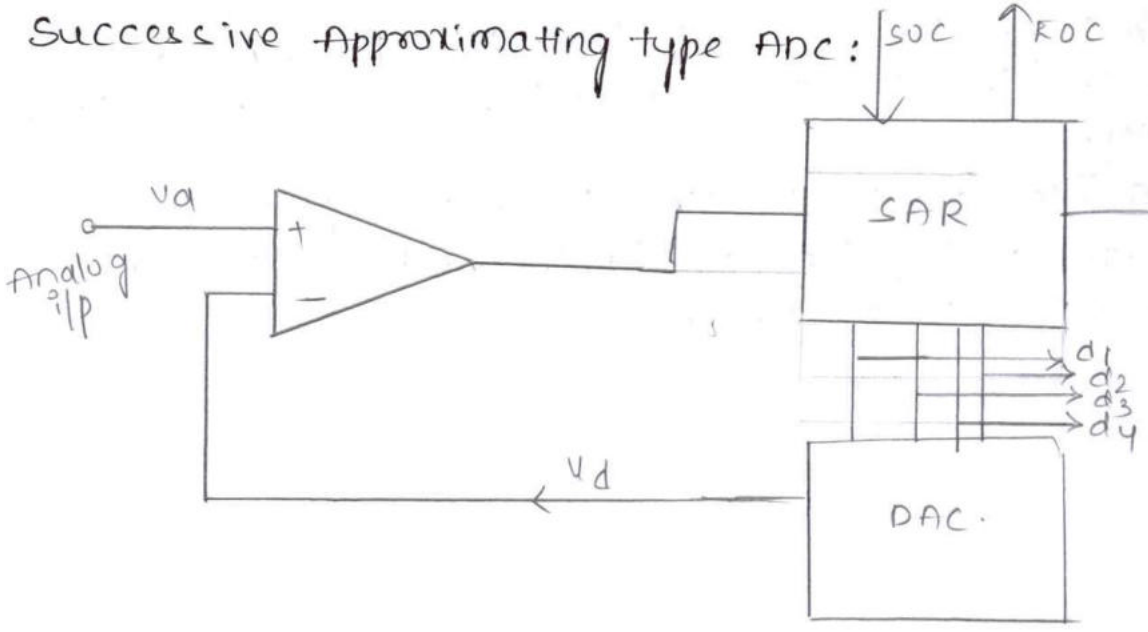
1. Initially the Counter is reset i.e its o/p set to zero by applying a reset pulse.
2. The output of Counter is given as digital input to DAC. Since input to DAC is zero its output is zero.
3. When the analog input is applied to Comparator, it becomes greater than V_0.
4. Here V_A is applied to the non-inverting terminal of the Comparator. When $V_A > V_D$ the Comparator o/p goes high.
5. For an "AND" gate one input is clock pulse applied and another input is the output of the Comparator.
6. When Comparator output is high there the AND gate is able to allow the clock pulses & it is given to the binary Counter.
7. The Counter starts counting these clock pulses according to the clock pulses goes on increasing. This increases the output of the DAC.

The above steps are repeated till $V_A < V_0$. When V_A is less than V_0 the output of comparator goes low due to these "AND" gate disables i.e AND gate is not allow the clock pulses so the Counting process of counter is stopped.

- for next A/D conversion the input voltage V_A changes. The binary Counter is cleared by applying second reset pulse.
- The corresponding wave form shown in below figure.

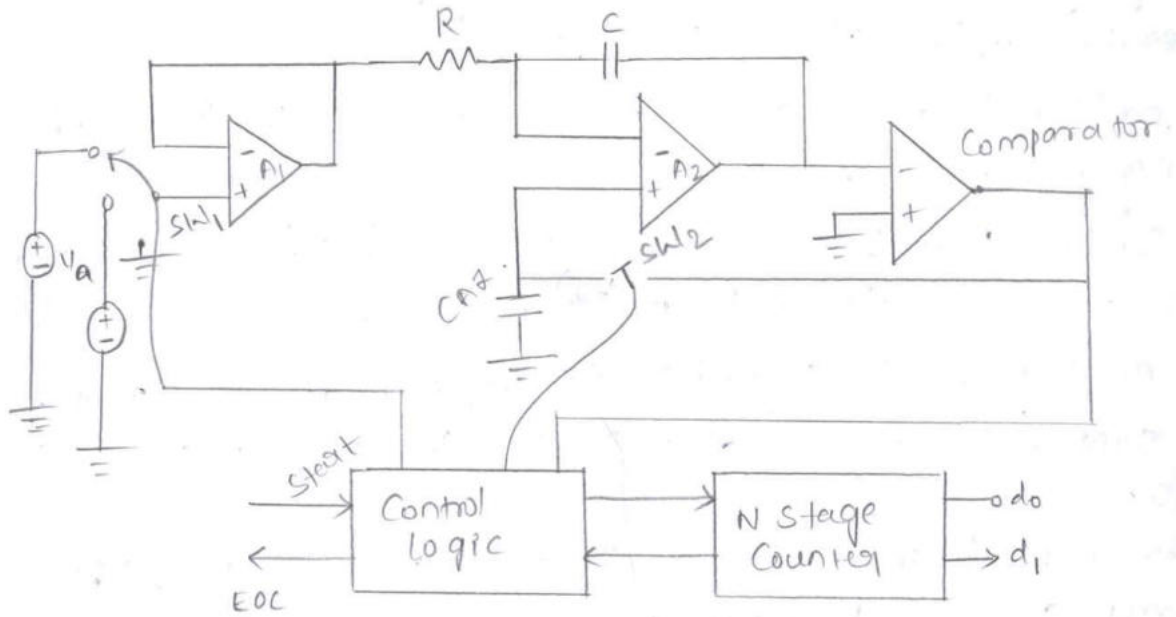


c) Successive Approximating type ADC:



- It Consists of SAR (Successive Approximation register), SOC, EOC and DAC, Comparator. (9)
- The successive approximation method uses for to search binary bits, it completes the searching process for n-bit conversion in 'n' clock cycles.
- The external clock signal is used to set the internal tuning parameters.
- The Control signal SOC is used to start the Conversion and EOC is used to end the Conversion.
- The Analog input signal v_a is applied at one input of the comparator before slot the SOC the output should be zero.
- After initializing the SOC, the SAR sets the four bit binary code as an input of DAC. i.e, its sets the MSB bit dial, while all other bits to zeros. So that the tarail code is 1000.
- Now the output of DAC is Compared with the analog input signal v_a.
- If $v_a > V_d$, the output of Comparator is one then the MSB bit (or) SCR sets the MSB bit left 1 and next LSB bit is made one and further tested.
- However if $v_a < V_d$, the output of Comparator is zero then SCR sets the MSB bit zero and next LSB bit is made one.
- This process repeated for all subsequent bits, one at a time until all bit positions have been tested.
- Whenever the DAC o/p crosses v_A, the Comparator changes the state and this can be taken as the EOC Control signal.

Dual Slope Type ADC:



- The above figure shows the dual slope type ADC.
- It consists of high input impedance buffer A_1, integrator A_2 and voltage comparator, Control logic & n-stage Counter.
- The Convertor first integrates the analog input signal V_a for a fixed duration of 2^n clock periods.
- Then it integrates on reference voltage V_R of opposite polarity until the integrator output is zero.
- The number of N clock cycles required to return the integrated to zero is proportional to the value of V_a average over the integration period.
- Before the start signal switch SW_1 is connected to ground and switch SW_2 is closed.
- So, any offset voltage present in the A_1 & A_2, it appears across the capacitor in C_{AZ} till the threshold of the Comparator is achieved. Thus the capacitor C_{AZ} is provides the input offset voltage of all the 3 amplifier.

- Later when SW_2 opens C_{A2} acts as memory device to store the energy levels (or) voltage.
- After START signal initiates at that, the control logic open SW_2 switch and SW_1 switch connects to the V_A and enables the counter starting from zero.
- Here n stage ripple counter is used so the counter resets to zero after counting 2^n clock cycles (or) pulses.
- If the clock period is t_1, the integration takes place for a time $t_1 = 2^n T$ and the output is a ramp going downward shown in below figure.
- The counter resets itself to zero at the end of the interval T and the switch SW_1 is connected to the reference voltage $-V_R$.
- Now, the output voltage V_a will have positive slope.
- However, when V_0 becomes just zero at a time $t = t_3$ the control logic issues an end of conversion signal. So, no further clock pulses enter the counter.
- It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

$$T = t_2 - t_1$$

$$= 2^n \cdot \frac{\text{Clock period}}{\text{clock pulses}}$$

$$t_3 - t_2 = n \cdot \frac{\text{clock cycles}}{\text{clock period}}$$

for an integrator

$$\frac{\Delta V_0}{\Delta V_t} = -\frac{1}{RC}$$

$$\Delta V_0 = -\frac{1}{RC} \Delta V_t$$

The voltages V_0 will be equal to V_1 at the instant t_2 and it can be written as

$$V_1 = -\frac{1}{RC} V_a (t_2 - t_1)$$

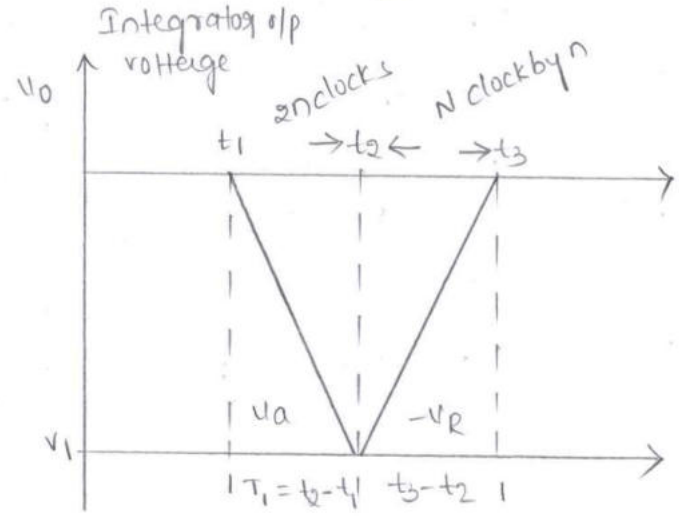
It can be also written as

$$V_1 = -\frac{1}{RC} V_R (t_3 - t_2)$$

$$V_a (t_2 - t_1) = -V_R (t_3 - t_2)$$

$$V_a (2^n) = -V_R (N)$$

$$V_a = \frac{-V_R (N)}{2^n}$$



Specifications of A/D and D/A Convertor:

1. Resolution.
2. Linearity.
3. Accuracy.
4. Setting Time
5. Stability.

Both A/D & D/A Convertors are available with wide range of Specifications.

- The various important Specifications of Convertor generally specified by the manufacture are analysing. (6)

Resolution:

The resolution of a Convertor is the Smallest change in voltage which may be produced at the output of the Convertor.

Linearity:

Linearity specification of Convertors. It is an important measure of accuracy and tells us how close the Convertor o/p is to its ideal transfer Characteristics.

Accuracy:

It is a maximum deviation between the actual Convertor (or) practical Convertor o/p to the ideal Convertor o/p.

Setting Time:

It represents the time it takes for the o/p of settle with in a specified band of its final value following a code Change at the input.

Setting ranges from 100 ns to 10ms depending upon word length and type of Circuit used.

Stability:

Stability shows the performance of the Convertor. The performance of Convertor changes the Temperature, age of Components, power supply variations.